2011 Single-Event Effects Symposium
Technical Program

12-14 April 2011

Monday, 11 April

- 5:00 – 8:00 PM Registration/Reception
- 5:00 – 9:00 PM Industrial Exhibit Setup

Tuesday, 12 April

- 7:30 – 8:30 AM Continental Breakfast
- 8:30 AM V. Ferlet-Cavrois Welcome and Local Arrangements
- 8:35 AM N. Haddad Introduction to Technical Program

Invited Talk

8:40 AM Reno Harboe Sørensen 40 years of SEE at ESA/ESTEC

Session A: Design and Process Hardening **Chair: K. Avery, AFRL/RVSE**

9:30 AM	D. F. Heidel, IBM Corp.	SEU Hardened SOI Latches
9:50 AM	R. W. Blaine, Vanderbilt University	A RHBD Bootstrap Current Source Utilizing Sensitive Node Active Charge Cancellation (SNACC)
10:10 AM	N. M. Atkinson, Vanderbilt University	Design Technique for Mitigation of Soft Errors in Transmission-Gate-Based Switched-Capacitor

10:30 – 11:00 AM Break

Session A: Design and Process Hardening **Chair: K. Avery, AFRL/RVSE**

11:00 AM	V. Bratov, ADSANTEC	I2C Digital Interface Block Based on a 130nm Radiation-Hardened CMOS Library
11:20 AM	P. Maillard, Vanderbilt University	A Radiation-Hardened Delay-Locked Loop Design Utilizing Differential Delay Line Topology
11:40 AM	P. Obiomon, Prairie View A&M Univ.	Layout Guidelines to Minimize Latchup in CMOS Circuits Using Guard Rings

12:00 – 1:00 PM Lunch

9:00 AM – 9:00 PM Industrial Exhibits Open
9:00 PM – 11:00PM Tear Down for Industrial Exhibits

Invited Talk

1:10 PM	Jeff Titus, NSWC/Crane	Update Perspective of SEB and SEGR in Power MOSFETs (tentative title)

Session B: Destructive Single-Event Effects **Chair: R. Harboe Sørensen, ESA-Ret.**

1:50 PM	T. R. Oldham, Dell-Perot Government Systems / NASA GSFC	Investigation of Current Spike Phenomena During Heavy Ion Irradiation in NAND Flash Memories
2:10 PM	S. Liu, International Rectifier	Effects of Ion Species on SEB Failure Voltage of Power DMOSFET
2:30 PM	R. L. Ladbury, NASA/GSFC	Challenges of Rate Estimation for Destructive and Disruptive Single-Event Effects

2:50 – 3:20 Break

Open Forum Panel Discussion **Moderator: P. McNulty, Clemson University**

3:20 - ??	Destructive Event Signatures in Flash Memories	NASA/GSFC, NASA/JPL-Caltech, ESA/ESTEC, University of Padova,

5:30-9:00 PM Reception and Industrial Exhibits

- **5:30-6:30 PM Cocktails and Appetizers**
- **6:30-9:00 PM Reception**

Wednesday, 13 April

- 7:30-8:30 AM Continental Breakfast

Session C: Single-Event Transients **Chair: M. Gadlage, NWSC-Crane**

8:30 AM	S. Buchner, Naval Research Laboratory	Comparison of Single Event Transients Generated by Pulsed Lasers at NRL, IMS, EADS and JPL
8:50 AM	P. Eaton, Micro-RDC	NBTI as the True Cause for DSET Pulse Broadening
9:10 AM	N. J. Gaspard, Vanderbilt University	Effect of Latchup Mitigation Techniques on Well Potential Modulation and Single-Event-Transient Pulse Widths
9:30 AM	N. D. Pate, Vanderbilt University	Application of Scattering Parameter De-Embedding to the Reconstruction of Single Event Transients
9:50 AM	H. Barnaby, Arizona State University	Analytical Model for Transient Radiation Effects in Floating Body SOI Transistors

10:10 – 10:30 Break

Invited Talk

10:30 AM	Reed Lawrence, BAE Systems	Single Event Effect Considerations in Test Methods and Standards under Review at JEDEC Meetings

Session D: Single-Event Test Methods **Chair: E. Cannon, Boeing**

11:00 AM	M. R. Shaneyfelt, Sandia National Labs	SOI Substrate Removal for SEE Characterization: Techniques and Applications
11:20 PM	R. Schwank, Sandia National Labs	Comparison of Single and Two-Photon Absorption for Laser Characterization of Single-Event Upsets in SOI SRAMs
11:40 PM	J. S. Buchner, Naval Research Laboratory	Variable Depth Bragg Peak Method For Single Event Effects Testing

12:00 – 1:00 PM Lunch

Session D: Single-Event Test Methods **Chair: W. Heidergott, General Dynamics**

1:10 PM	D. McMorrow, Naval Research Laboratory	Single-Event Effects Induced by Two-Photon Absorption: Recent Results and Developments
1:30 PM	M. P. King, Vanderbilt University	The Implications of Ion Track Structure for Single-Event Effect Analysis
1:50 PM	V. Ferlet-Cavrois, ESA/ESTEC	Influence of beam conditions and energy for SEE testing of power MOSFETs, analog and digital components
2:10 PM	J. A. Pellish, NASA/GSFC	Low-Energy Proton Testing Using Cyclotron Sources

Session E: Product & Technology Evaluation **Chair: M. Shoga, Consultant**

2:30 PM	K. Lilja, Robust Chip Inc.	Predictive Analysis, Comparisons, and Optimization of Single Event Soft Errors in Flip-Flops at 40nm and 28nm Technology Nodes
2:50 PM	H. Puchner, Cypress Semiconductor	Comprehensive Radiation Study of a High Speed 72Mbit Quad Data Rate SRAM for Space Applications

3:10 – 3:40 Break

Session E: Product & Technology Evaluation Chair: M. Shoga, Consultant

3:40 PM	S. Armstrong, NSWC-Crane/Vanderbilt University	Single-Event Vulnerability of Multi-Protocol, Multi-Feature Communications Devices
4:00 PM	P. E. Dodd, Sandia National Labs	SEU Sensitivity and Distributions in CMOS Flip-Flops
4:20 PM	P. McNulty, Clemson University	When Are Soft Errors Not Single-Event Effects?
4:40 PM	S. Guertin, NASA/JPL-Caltech	Testing for Rare SEEs in Fault Tolerant Devices

6:00 PM - 8:00 PM Happy Hour

Thursday, April 14

- 7:30 - 8:30 AM Continental Breakfast

Session F: Single-Event Test Facilities **Chair: E. Cannon, Boeing**

8:30 AM	V. Skuratov, Joint Institute for Nuclear Research	Roscosmos Ion Beam Line for SEE Testing at U400M FLNR JINR Cyclotron
8:50 AM	G. R. Allen, NASA/JPL-Caltech	Current Status of the Jet Propulsion Laboratory's Pulsed Laser Facility

Session G: FPGAs **Chair: S. Rezgui, Microsemi**

9:10 AM	M. D. Berg, MEI Technologies-NASA/GSFC	The Evaluation of Combinatorial Logic and Routing Affects to Single Event Transient Propagation in the Actel RTAXs FPGA
9:30 AM	C. Carmichael, Xilinx Inc.	SEE Characterization and Recovery Mechanisms of MGTs in Space-grade Virtex-5 FPGAs
9:50 AM	V. Liberali, University of Milano	Impact of Placement on SEU Sensitivity in SRAM-based FPGA

10:10 – 10:30 Break

Session G: FPGAs **Chair: S. Rezgui, Microsemi**

10:30 AM	R. Monreal, Southwest Research Institute	Single-Event Characterization and Mitigation Techniques of DSPs Embedded in Space-Grade FPGAs
10:50 AM	G. Swift, Xilinx Inc.	Techniques for Identifying SET Sources with Examples from Virtex-5QV Testing
11:10 AM	S. Rezgui, Microsemi Corp.	First SEE Characterization of the Analog Block of the 0.13 μm Fusion Mixed-Signal Flash-Based FPGA

11:30 AM End of Technical Session

2:00 PM Volleyball Session **Chair: Dale McMorrow, NRL**