An Evaluation of Transistor-Layout RHBD Techniques for SEE Mitigation in SiGe HBTs

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***Abstract*—We investigate transistor-level layout-based techniques for SEE mitigation in advanced SiGe HBTs. The approach is based on the inclusion of an alternate reverse-biased *pn* junction (n-ring) designed to shunt electron charge away from the sub-collector to substrate junction. The inclusion of the n-ring affects neither the *dc* nor *ac* performance of the SiGe HBT and does not compromise its inherent multi-Mrad TID tolerance. The effects of ion strike location and angle of incidence, as well as n-ring placement, area, and bias on charge collection are investigated experimentally using a 36 MeV O_2 microbeam. The results indicate that charge shunting through the n-ring can result in up to a 90% reduction in collector collected charge for strikes outside the DT and a 18% reduction for strikes to the emitter center. 3-D transient strike simulations using NanoTCAD are used to verify the experimental observations, as well as shed insight into the underlying physical mechanisms. Circuit implications for this RHBD technique are discussed and recommendations made.**

***Index Terms*—Charge collection, deep trench (DT), ion beam induced charge collection (IBICC), NanoTCAD, radiation hardening by design (RHBD), silicon-germanium (SiGe), SiGe HBT, single event effects (SEE).**

I. Introduction

SiGe BiCMOS is rapidly evolving as a key technology enabler for extreme environment electronics, as a result of its built-in multi-Mrad (SiO_2) total ionizing dose (TID) tolerance, enhanced performance at cryogenic temperatures, high-level integration capability, and low cost [1]. Single event effects (SEE) mitigation continues to be a major research area in SiGe, with recent results demonstrating limiting cross-sections (SEU-free operation) at linear energy transfer (LET) values well above 50 MeV-cm^2/mg for 16-bit shift registers [2]. This milestone was achieved by first dual-interleaving the pass and storage cells of the latch, followed by the subsequent encapsulation of the register in triple modular redundancy (TMR) architecture with voting at end (VAE) decision blocks with the associated area and/or power consumption penalties [3]. In the present work, a radiation hardening by design (RHBD) technique implemented solely using transistor layout variations to the standard SiGe HBT is proposed. This transistor-level RHBD approach targets bulk SiGe HBTs without any intentional process-induced hardening.

Drift transport of excess carriers (generated in the aftermath of a heavy ion strike) via the strong electric field of a reverse biased *pn* junction has long been accepted as the primary mechanism for charge collection in semiconductor devices [4], [5]. In the SiGe HBT, the junction of interest is the substrate (p) to sub-collector (n) junction, which is universally reverse-biased in normal circuit operation. 3-D TCAD simulations of charge collection in SiGe HBTs have identified the collector and emitter terminals as the sink for electrons, and the base and substrate as the sink for holes, in the case of an *npn* SiGe HBT. The relative contributions from each terminal depend strongly on the loading characteristics (terminal impedances), bias, substrate doping, and ion strike depth [6], [7]. Perturbations in the collector node voltage resulting from electrons collected at the collector of the device and coupled into the loaded circuit have also been identified as the primary mechanism underlying the observed broad-beam heavy ion circuit sensitivity [8] first reported in [9].

The RHBD approach presented here features an alternative/additional route to SEE hardening in SiGe HBTs, by implementing a low impedance path within the transistor designed to shunt charge away from the collector terminal. This path is realized by including an additional reverse biased *pn* junction formed between the p-substrate and n^+ guard ring (n-ring) resulting in a secondary electric field. Special considerations in the implementation of this approach include: the location and area (A_{NR}) of the n-ring; n-ring bias (V_{NR}); enclosed trench area (A_{DT}); strike location, and incident angle (θ).

Manuscript received July 20, 2007; revised September 5, 2007. This work was supported in part by the Defense Threat Reduction Agency (DTRA) under the Radiation Hardened Microelectronics Program, in part by the NASA Goddard Space Flight Center (GSFC) under the NASA Electronic Parts and Packaging (NEPP) Program, in part by the NASA Exploration Technology Development Program (ETDP), in part by the AFOSR Multidisciplinary University Research Initiative (MURI) program, in part by Sandia National Laboratory, and in part by the Georgia Electronic Design Center (GEDC) at the Georgia Institute of Technology.

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Digital Object Identifier 10.1109/TNS.2007.908697

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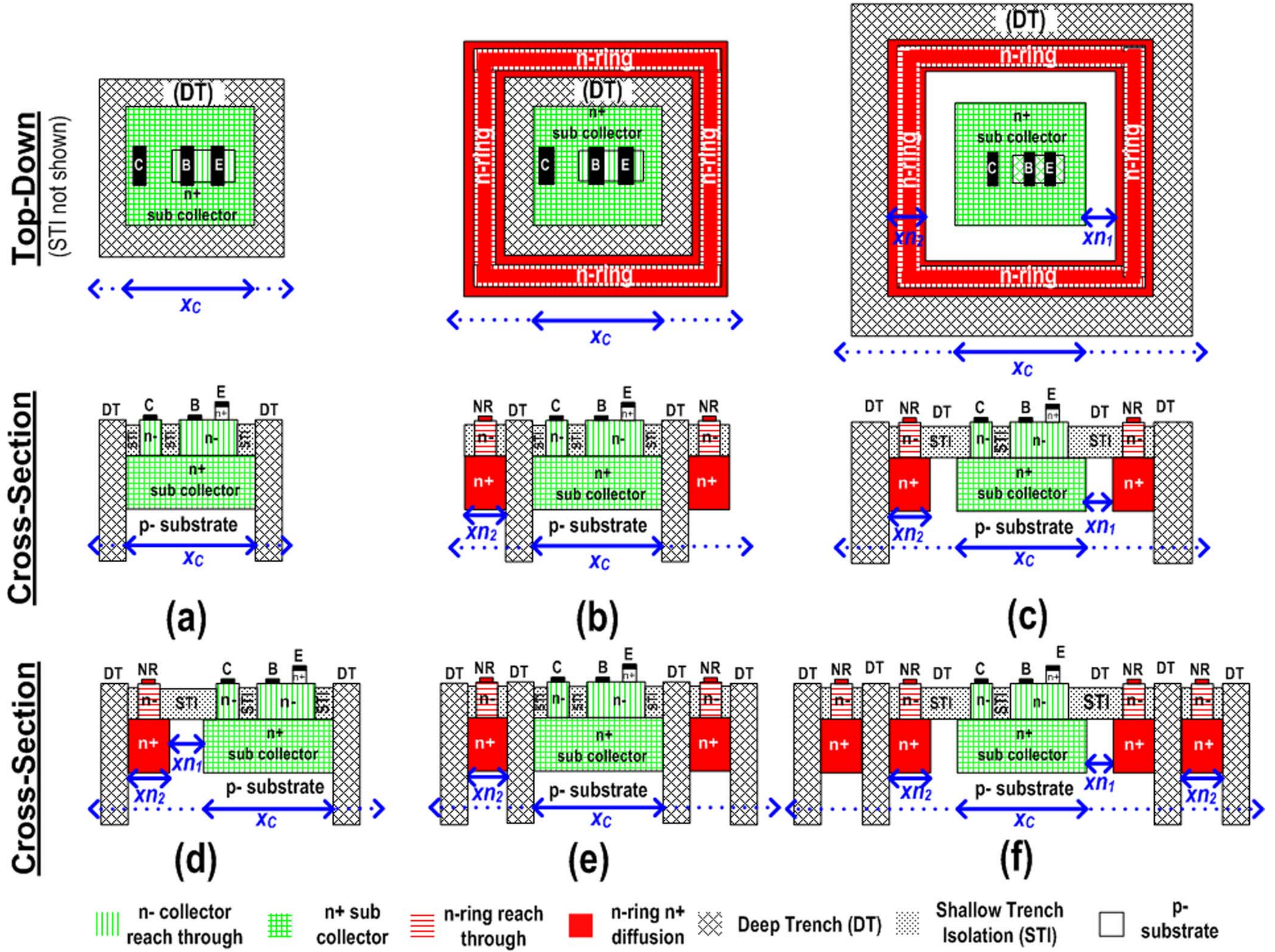

Fig. 1. Top down and cross-section views of the: (a) nominal-HBT (unhardened); (b) external R-HBT; (c) 3, 6, 8 μm R-HBT; and cross-section views of the (d) 1-sided 3 μm R-HBT, (d) 1NR, 2DT (3 μm R-HBT) (f) 2NR, 2DT (3 μm R-HBT). The key lateral dimensions x_C, xn_1 and xn_2 are shown.

II. Devices Under Test

A. RHBD Layout Variations

The SiGe HBT evaluated in this work features an $f_T/f_{\rm MAX}$ of 200/285 GHz, a $BV_{\rm CEO}$ of 1.7 V, and is offered alongside 130 nm CMOS in the commercially-available IBM 8 HP, seven metal layer (7 LM) SiGe BiCMOS process [10]. The device is fabricated on an 8–10 Ω-cm p-type substrate with an *in-situ* doped polysilicon emitter, raised extrinsic base, a conventional (5 to 7 μm) deep-trench (DT), and shallow-trench (ST) isolation. All devices are implemented in a single stripe CBE configuration, as opposed the larger double-collector, double-base stripe CBEBC configuration, featuring an emitter area (A_E) of 0.12×3.0 μm^2. The CBE configuration has a smaller internal trench area as discussed in [2]. The top down and cross section views of RHBD layout devices featuring a variety of n-ring placement and spacing are shown in Fig. 1(a)–(f). The lateral distance across the device is denoted as x_C, the width of the n-ring is denoted as xn_2, and the spacing between the internal n-ring and the device sub-collector is denoted as xn_1. The devices tested feature an n-ring width of 2 μm and a spacing varying from 3 to 8 μm. In the 8 HP process, a spacing less than 3 μm could result in an n-ring to sub-collector short as a result of dopant out-diffusion during device fabrication. A smaller n-ring spacing, allowing for a more compact and effective design, may be possible in other technology platforms with reduced doping levels. In this work we focus on the measured and simulation charge collection of the nominal-HBT, external R-HBT and the internal 3 μm R-HBT which have shown to be the most effective in SEE mitigation. Measured charge collection of alternate n-ring schemes such as the 1-sided 3 μm R-HBT (reduced $A_{\rm DT}$), 1 NR, 2 DT 3 μm R-HBT (external R-HBT + 2nd outside DT), and 2 NR, 2DT 3 μm R-HBT (internal + external R-HBT devices with a 2nd outside DT) are used to understand the charge collection dynamics.

The inclusion of the n-ring in the device layout affects neither the *dc* nor *ac* performance of the device (regardless of the applied V_{NR} or xn_1), as evidenced by the overlay of the forward-mode Gummel and f_T versus I_C characteristics shown in Fig. 2(a) and (b). In the case of the internal R-HBT devices, the maximum applicable V_{NR} (occurring when the substrate to n-ring depletion region contacts the device sub-collector) is proportional to xn_1, being reduced from 25 V at $xn_1 = 8$ μm to 9 V at $xn_1 = 3$ μm, for $V_C = V_B = V_E = 0$ V.

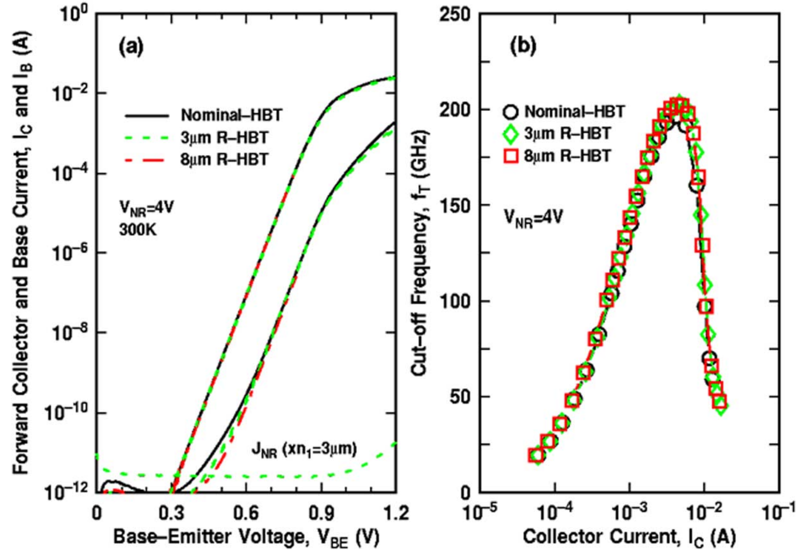

Fig. 2. RHBD impact on device performance: (a) Forward-mode Gummel comparison for the nominal-, 3 μm-and 8 μm R-HBT devices and, (b) f_T versus I_C characteristics of the nominal 3-and 8-μm R-HBT devices.

B. Experiment Details

Total ionizing dose (TID) tolerance of the 8 μm R-HBT device was evaluated via proton testing at the Crocker Nuclear Laboratory, the dosimetry system of which has been previously described in [11], [12]. Irradiations were performed to a cumulative dose of 3 Mrad (SiO_2) for $V_{NR} = \pm 3$ V with all device terminals grounded. The post-irradiation ΔJ_B for the 8 μm R-HBT is comparable to that of the nominal-HBT, indicating that TID tolerance has been maintained. This result follows from the fact that the inclusion of the n-ring does not alter the location of the emitter-base (EB) spacer and shallow trench isolation (STI) Si/SiO_2 interfaces, where radiation induced interface trap density $(D_{\rm it})$ is expected to be highest [13].

Ion microbeam testing was performed at Sandia National Laboratory's ion beam induced charge collection (IBICC) facility [14]–[16]. 36 MeV ^{16}O ions, with a 1 μm spot size, a range of 25.5 μm in Si, surface LET of 5.2 MeV-cm^2/mg and a Bragg peak of 7.5 MeV-cm ^{2}/mg were stepped across a 100×100 μm^2 field encompassing the device active area. Charge collection on the 5 terminals (C, B, E, SX and NR) were monitored for $\theta = 0°$ and 15° strikes. Prior to ion exposure, a non-destructive, fluorine-based reactive ion etch (RIE) was used to selectively remove several microns of inter-metal dielectric above the device, thereby increasing charge deposition in the substrate underlying the device active area. There was no measured degradation in the device performance characteristics.

III. Microbeam Results

The 3-D charge collection data was reduced by taking a 1 μm wide slice in the y-axis direction about the peak collector collected charge (Q_C) in the x-y plane and projecting it onto the x-axis (x_C in Fig. 1). A 1 μm slice was chosen to avoid sampling too many external DT events (slice widths >1 μm), and not capturing the charge collection profile (slice widths <1 μm). The peak Q_C and the path integral of Q_C along x_C ($Q_{C,\rm INT}$) in (1) will be used as the key performance figure-of-merit for comparing the SEE mitigation capability of the various RHBD layout schemes. The peak Q_C is representative of collection resulting from an emitter center strike, whereas $Q_{C,\rm INT}$ is representative of the sum of the collection resulting from strikes across the entire length (x_C) of the 1 μm slice

$$Q_{C,\rm INT} = \int_a^b Q_C(x_C)dx_C. \quad (1)$$

Q_C is illustrated as a function of x_C, for the nominal-, 8 μm, 3 μm-, and external-HBT devices at $V_{NR} = 4$ V and $\theta = 0°$ in Fig. 3. 36 MeV ^{16}O ions deposit 26 MeV of energy, generating 1.1 pC of charge in Si. Prior investigations (on IBM 7 HP), have determined a peak Q_C of approximately 1.0 pC, representing a 90% charge collection efficiency [17]. A normal incident emitter center strike will result in the largest amount of charge deposition, thereby corresponding to the observed peak Q_C. The nominal-HBT has a peak Q_C of 0.95 pC for strikes within the DT and over 0.1 pC of collector collection for external DT strikes. For the internal R-HBT device there was no observed reduction in the peak Q_C at 8 μm; however, as x_{n1} is scaled down to 3 μm, a slight reduction in peak Q_C is observed. The external R-HBT offers no immunity for strikes inside the DT but does an excellent job at reducing collection from external DT strikes.

A. N-Ring Bias

The value of V_{NR} for a given V_{SX} determines the reverse bias voltage of the substrate to n-ring junction and consequently the depletion width, electric field, electrostatic potential, and ultimately the drift-dominated charge collection volume. The path integrated collected charge for all device terminals as a function of V_{NR} is illustrated in Fig. 4(a) and (b) for the 3 μm R-HBT and external R-HBT, respectively. As expected from prior investigations [17] negligible charge collection is observed on the base and emitter. Charge collection on the remaining terminals is balanced ($Q_{C,\rm INT}+Q_{NR,\rm INT} = Q_{SX,\rm INT}$). Increasing V_{NR} yields a noticeable increase in $Q_{NR,\rm INT}$ and $Q_{SX,\rm INT}$ together

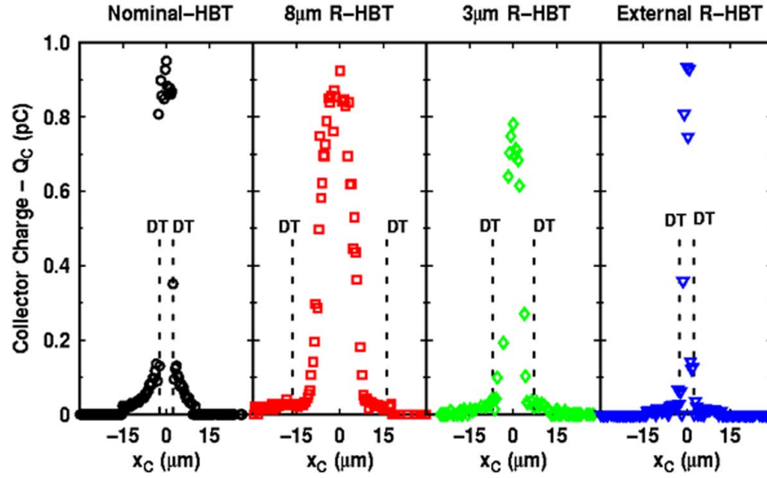

Fig. 3. Q_C as a function of x_C for the (a) nominal, (b) 8 μm, (c) 3 μm, and (d) external R-HBT. $V_{NR} = 4$ V for all R-HBT devices.

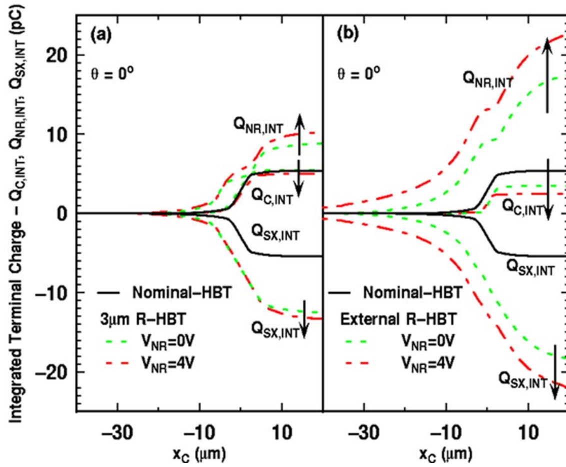

Fig. 4. Path integrated terminal charge ($Q_{C,\mathrm{INT}}, Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) 3 μm R-HBT and (b) external R-HBT for $V_{NR} = 0$ and 4V and $\theta = 0°$.

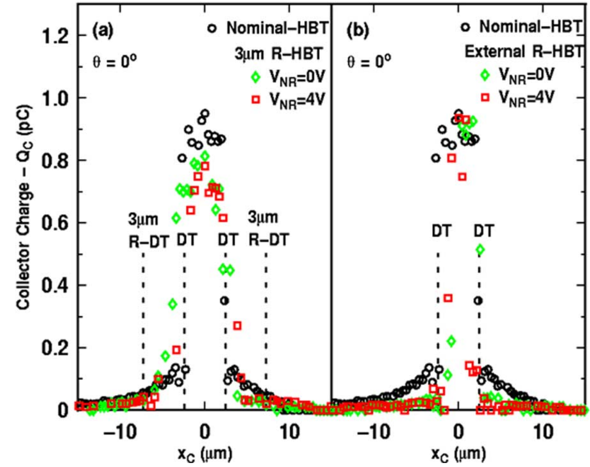

Fig. 5. Q_C as a function of x_C and V_{NR} for the (a) 3 μm R-HBT and (b) external R-HBT at $\theta = 90°$.

with a slight decrease in $Q_{C,\mathrm{INT}}$. The external n-ring collects approximately 2X more charge than the 3 μm internal ring, and demonstrates a larger percentage increase in $Q_{NR,\mathrm{INT}}$ as V_{NR} is increased. Q_C is depicted as a function of x_C at $V_{NR} = 0$ and 4 V for the 3 μm R-HBT and external R-HBT as shown in Fig. 5(a) and (b), respectively. Although the external n-ring collects 2X more charge than the 3 μm R-HBT, it offers no mitigation for emitter center strikes, while the 3 μm internal ring at $V_{NR} = 4$ V yields an 18% reduction in peak Q_C. Moreover, changes in V_{NR} have very little effect on the peak Q_C for both the internal and external ring devices.

B. Strike Location and Angle of Incidence

In addition to V_{NR}, the strike location (relative to the DT) and angle of incidence, θ, also impact the observed charge collection. Q_C is plotted on a logarithmic scale as a function of x_C for the nominal-, 3 μm R-HBT and external R-HBT devices at $V_{NR} = 4$ V for $\theta = 0°$ and 15° in Fig. 6(a) and (b), respectively. A strike through the center of the emitter presents the largest volume for charge deposition and un-recombined carriers are efficiently collected via drift and funneling [5]. Strike locations on the outside of the DT generate electron-hole pairs that must first diffuse under the DT before they can be collected via drift, resulting in a Q_C that is at least an order of magnitude smaller. The external n-ring provides up to 90% reduction in Q_C from strikes originating in this region, while the 3 μm ring device provides only a small reduction.

The nominal-HBT, external R-HBT, and 3 μm R-HBT all yield approximately 20% reduction in observed in peak Q_C for internal DT strikes and an increasingly asymmetric external DT collection component when θ is increased from 0° to 15°. External DT collection is also reduced, as evidenced by a rapidly decaying Q_C in the case of the nominal- and 3 μm R-HBT, and complete suppression for the external R-HBT as shown in Fig. 6(b). At $\theta = 15°$, $Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$ are also reduced (when compared to $\theta = 0°$), as illustrated in Fig. 7(a) and (b).

The effective LET, described by the inverse cosine law, $(\mathrm{LET_{eff}} = \mathrm{LET_0}/\cos\theta)$ has traditionally been used to model enhanced charge collection at large θ. There have been, however, several experimental results that contradict the validity of

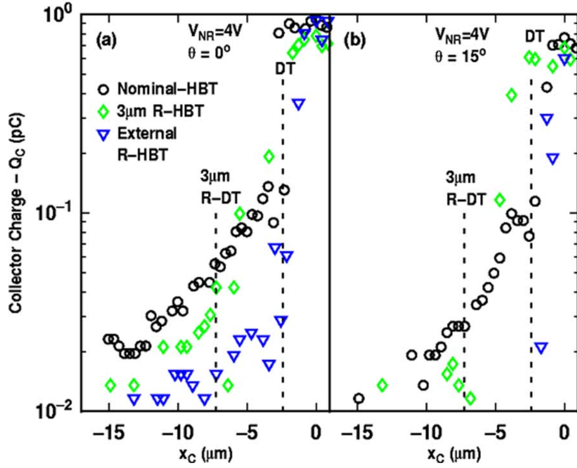

Fig. 6. External DT collection for the nominal-HBT, 3 μm R-HBT, and external R-HBT for $V_{NR} = 4$ V at (a)$\theta = 0^{\circ}$ and (b) $\theta = 15^{\circ}$.

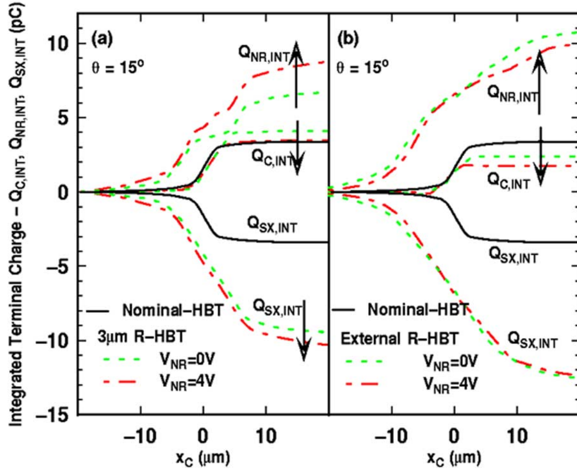

Fig. 7. Path integrated terminal charge ($Q_{C,\mathrm{INT}}, Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) 3 μm R-HBT and (b) external R-HBT for $V_{NR} = 0$ and 4 V and $\theta = 15^{\circ}$.

this model, as discussed in [18] for the case of CMOS SRAMs. In the case of the 7 LM 8 HP process used here, a larger θ translates into an increased path length in the over-layer material, resulting in reduced ion energy (and charge deposition) in the substrate. Additionally, perturbation of the ion track through the DT may contribute to reduced internal DT collection.

C. Alternate N-Ring Schemes

One of the major drawbacks of the internal ring structure is the increase in the enclosed trench area (A_{DT}), and resulting increase in the drift dominated charge collection volume. To further reduce A_{DT}, the ring may be converted into a single- or double-tap structure, as illustrated in Fig. 1(d). Although A_{DT} is now smaller, these structures suffer from a reduction in the total n-ring area, and the resultant $Q_{NR,\mathrm{INT}}$ is reduced by almost 90% compared to the 3 μm R-HBT, as shown in Fig. 8(a). In this case the substrate to collector junction area is larger than the substrate to n-ring junction area, resulting in an increased $Q_{C,\mathrm{INT}}$. Charge balance is still maintained $(Q_{C,\mathrm{INT}} + Q_{NR,\mathrm{INT}} = Q_{SX,\mathrm{INT}})$

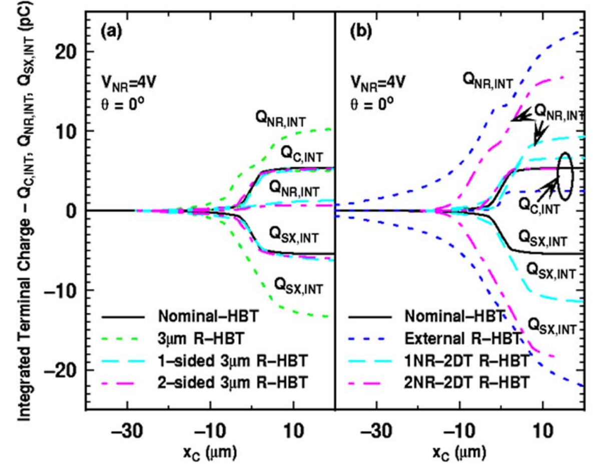

Fig. 8. Path integrated terminal charge ($Q_{C,\mathrm{INT}}, Q_{NR,\mathrm{INT}}$, and $Q_{SX,\mathrm{INT}}$) for the (a) reduced A_{DT} devices: 1-, 2-sided 3 μm R-HBT compared to 3 μm R-HBT and (b) double DT devices: 1NR-2DT R-HBT and 2NR-2DT R-HBT compared to external R-HBT. All comparisons at $V_{NR} = 0$ and 4 V and $\theta = 0^{\circ}$.

The external R-HBT has demonstrated the largest reduction in external DT collection, but little mitigation in the event of an emitter center strike. The substrate to n-ring junction for this device is not bounded by DT, thereby enabling both vertical and lateral collection. Encapsulation of this external ring [i.e., going from Fig. 1(b) to Fig.1(e)] by a 2nd DT results in over 50% reduction in $Q_{NR,\mathrm{INT}}$, as shown in Fig. 8(b), as much of the lateral directed drift collection is now shut down. An obvious approach would be to combine external and internal rings in the same device. This is the case for the 2NR-2DT shown in Fig. 1(f). As shown in Fig. 8(b), $Q_{NR,\mathrm{INT}}$ increases significantly for this device with a corresponding decrease in peak $Q_{C,}$ and $Q_{C,\mathrm{INT}}$ approximately equal to that of the 3 μm R-HBT device, but at a 2X area penalty.

A summary of the observed charge collection is presented in Table I. In addition to peak Q_C and $Q_{C,\mathrm{INT}}$, the charge collected for strikes approximately 1 μm outside of the DT (the bounding trench for that specific device) is also tabulated (Q_C (DT+1)). As shown previously, the inclusion of the external n-ring results in a 90% reduction in the collected charge from events outside of the trench. This is the driving force behind the 53% reduction in the overall $Q_{C,\mathrm{INT}}$ for the external R-HBT (the best out of all devices tested). The addition of a 2nd DT on the outside of this structure [i.e., Fig. 1(e)] slightly reduces the advantage to 85% (although now events outside the trench are further away from the sub-collector).

IV. Charge Collection Simulations

3-D charge collection simulations were performed using the NanoTCAD simulation package [19], which has been previously been used to simulate radiation effects on a range of modern IC technologies [20]–[22]. Layout information, from substrate through to 1st level metal, was imported from Cadence, into a meshing utility, in GDS II format. Next, a solid geometry model of the transistor was constructed using a binary tree mesh represented as a $26 \times 26 \times 25$ μm^3 volume with local refinement of the mesh in the vicinity of

TABLE I
CHARGE COLLECTION FOR ALL DEVICES AT $\theta = 0^\circ$ AND 15°

Device	A_{DT} (μm²)	A_{NR} (μm²)	Q_C *(E)* (pC)	Q_C (DT+1) (pC)	$Q_{C,INT}$ (pC)
Nominal-HBT	11	NA	0.950	0.133	5.34
3 μm R-HBT	172	29	0.781	0.017	3.16
6 μm R-HBT	363	43	0.888	0.039	9.55
8 μm R-HBT	972	54	0.924	0.027	11.63
External R-HBT	11	59	0.935	0.012	2.48
1-sided R-HBT	24	1.2	0.878	0.115	5.36
2-sided R-HBT	37	2.4	0.845	0.102	5.36
1NR-2DT	69	16	0.978	0.021	6.68
2NR-2DT	326	68	0.749	0.020	5.33
at $\theta = 15^\circ$					
Nominal-HBT	11	NA	0.766	0.051	3.38
3 μm R-HBT	172	29	0.679	0	3.46
External R-HBT	11	59	0.602	0	1.74

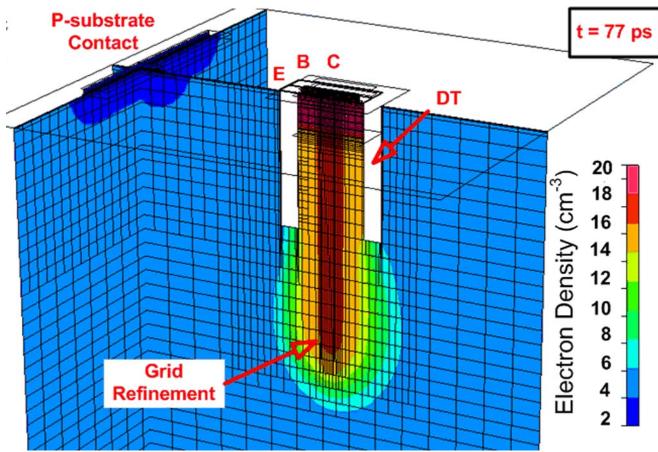

Fig. 9. X-cut through a 3-D solid geometry mesh of the nominal-HBT showing the electron density 77 ps following an emitter center strike.

the ion strike, as shown in Fig. 9. The EB spacer and DT oxide volumes were not meshed. In order to maintain such a relatively small volume (to be computationally efficient), and avoid reflective boundary conditions at the edges (which is non-physical), a "wrapping layer" with an artificially low lifetime ($\tau_{WR} = 50$ ns), encased the entire substrate volume. A standard substrate lifetime of 9 μs was used throughout the bulk region. Secondary ion mass spectroscopy (SIMS) data was used to reproduce the doping profiles, which are represented as a series of rectangular well regions with a constant dopant density enclosed by Gaussian distributed tails along the edges. Physical 3-D device models included doping-dependent carrier lifetimes, SRH and Auger recombination, and mobility models which accounted for doping, electric field and carrier-carrier scattering dependences.

Ion strike simulations were performed using a two step approach. First, steady-state conditions were established by the specification of initial boundary and volume conditions, and solution physics specific to the problem. Next, a transient ion strike simulation was performed using the steady-state solution as an initial condition. Normally incident ions were simulated at an LET of 0.07 pC/μm, a range of 13.72 μm (to account for 8 μm of dielectric), and Gaussian-distributed charge track peaking at 2 ps and with a *1/e* characteristic time scale of 0.25 ps and radius

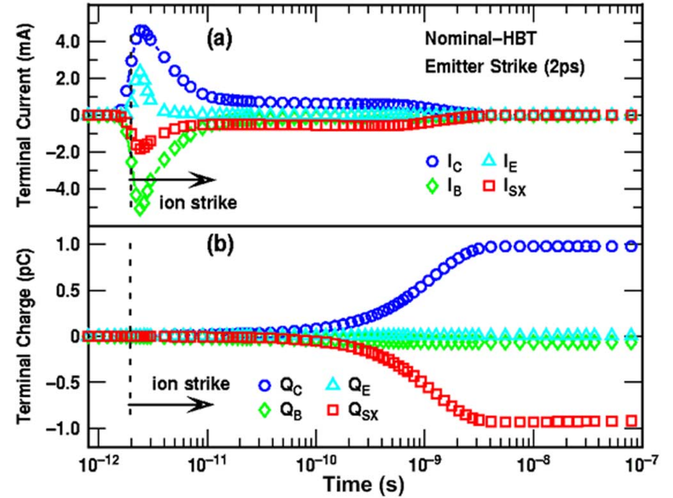

Fig. 10. Transient simulation results for an emitter centered ion strike to the nominal-HBT: (a) currents (I_C, I_B, I_E, I_{SX}), (b) charge (Q_C, Q_B, Q_E, Q_{SX}).

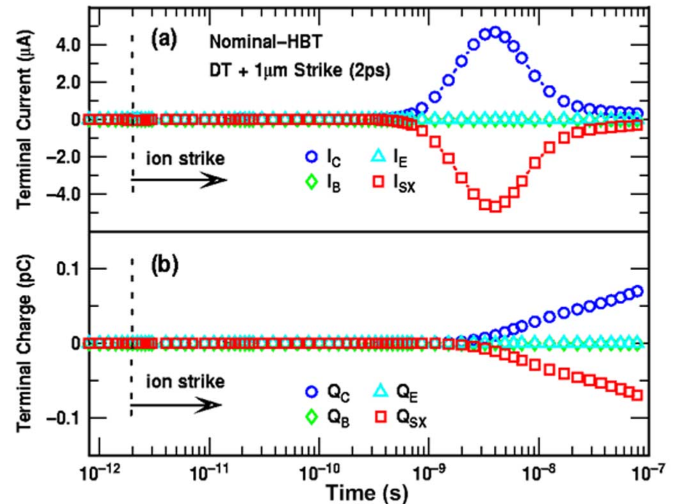

Fig. 11. Transient simulation results for an external DT ion strike to the nominal-HBT: (a) currents (I_C, I_B, I_E, I_{SX}), (b) charge (Q_C, Q_B, Q_E, Q_{SX}).

of 0.1 μm. To account for the potential impact of TID on charge collection, interface traps ($D_{\mathrm{IT}} = 5 \times 10^{11}$ cm^{-2}) were placed along all SiO_2 interfaces. Trap densities that were typical for studying TID effects in BJTs [23] were selected to match experimental charge collection data. Ion strikes on the external R-HBT and 3 μm R-HBT devices utilized similar model parameters as the nominal-HBT, with the exception that the lateral size of the 3-D model was extended to 40×40 μm^2. NanoTCAD was used to solve the fundamental carrier continuity and Poisson equations using the finite volume numerical method and post-processing performed using CFD-View. A typical ion strike simulation (to $10 +$ μs) takes 3 hours on a 2.4 GHz Pentium PC.

Transient terminal current charge collection profiles from a normal-incident ion strike at 2 ps through the emitter center, and through the external DT, are shown in Figs. 10 and 11, respectively. The current waveforms are composed of a 5–10 ps long prompt component soon after the strike (drift dominated), followed by a time-delayed component (diffusion dominated)

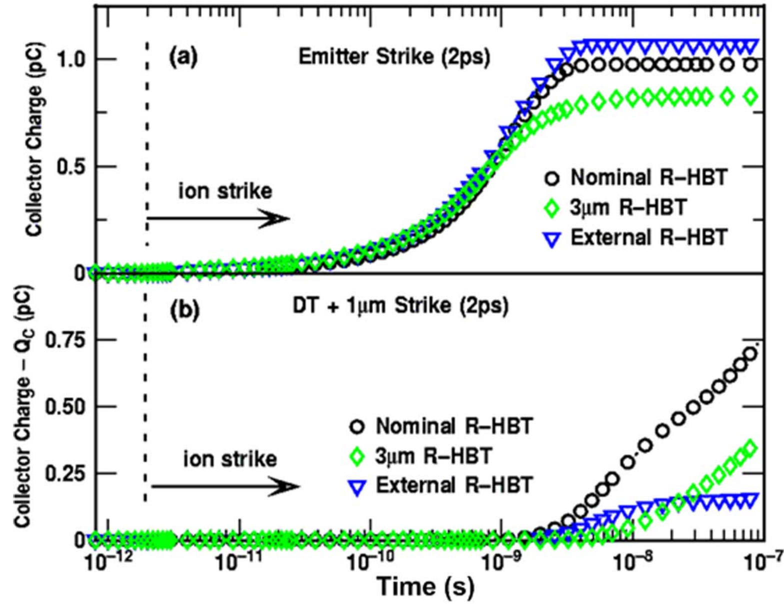

Fig. 12. Transient simulation results for nominal-, 3 μm R-, and external R-HBT showing Q_C (a) emitter centered (b) external DT strikes.

lasting up to 2 ns after the strike, as shown in Fig. 10(b). Prompt collection is observed on all terminals; however, delayed collection is only observed on the collector (electrons) and substrate (holes) terminals, which account for the majority of the collected charge, as shown in Fig. 10(b). These results are in reasonably good agreement with 3-D DESSIS ion strike simulations on 8 HP SiGe HBTs presented in [7] and [24]. In Fig. 11(a) an external DT strike result is shown to produce a delayed collection component observed only on the collector and substrate terminals. The peak of this delayed current component is observed 3–4 ns after the strike and is three orders of magnitude less than the prompt current component resulting in 0.07 pC collected after 100 ns (as opposed to 1 pC for the prompt current component), as shown in Fig. 11(b).

Transient Q_C for the nominal-HBT are compared with those of the 3 μm and external R-HBT devices, for an emitter center and external DT ion strike, as shown in Fig. 12(a) and (b). The inclusion of the substrate to n-ring junction results in the creation of a parasitic n(*collector*)-p(*substrate*)-n(*n-ring*) transistor. Under steady-state conditions ($V_{SX} = -4$ V, $V_{NR} = 0, 4$ V, $V_C = 0$ V), this device is in cut-off mode as both *pn* junctions are reverse-biased. In the aftermath of an ion strike, however, potential contours in the local vicinity of the strike are such that this parasitic BJT can be turned on (up to 0.5 ns after the strike) enabling a direct conduction path from the n-ring to the collector ($I_{NR} < 0$). In the case of the external DT strikes, the parasitic current flow is now from the collector to the n-ring ($I_{NR} > 0$) and also lasts up to 0.5 ns. A comparison of the measured and simulated Q_C is shown in Fig. 13(a) and (b), respectively. Each simulated Q_C represents a transient current integral over 14 μs. There is reasonably good agreement for drift-dominated strikes in the interior, while for strikes outside the DT there is some deviation between the simulated and measured results. Additional factors to consider include charge funneling

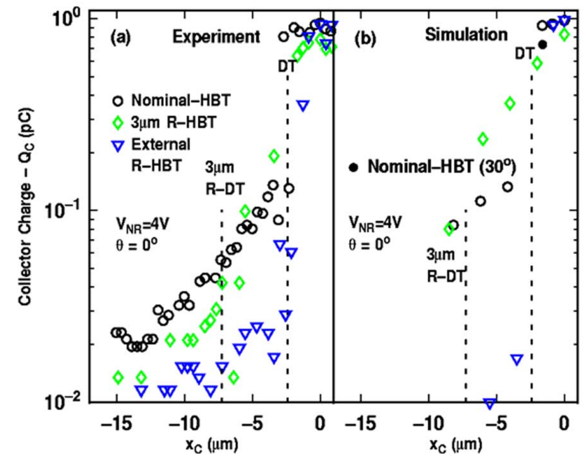

Fig. 13. Comparison of (a) experimental and (b) simulation results of Q_C as a function of x_C for the nominal-, 3 μm R-, and external R-HBT.

collection and the impact of secondary particles generated from nuclear interactions within overlaying metallization.

V. Discussion

An experimental evaluation of several layout-based RHBD techniques for SEU mitigation in SiGe HBTs has been presented and confirmed using 3-D transient ion strike simulations. In the best case scenario, reductions of 53% in $Q_{C,\mathrm{INT}}$ and 21% in peak Q_C have been demonstrated on two different R-HBT structures. These values compare well with the reductions achieved via employing varying epitaxial thicknesses [25], but are substantially lower than the reductions achieved via putting the SiGe HBTs on SOI [26], and ultimately still result in Q_C values much larger than the typical critical charge ($Q_{\mathrm{crit}} = 100$ fC) determined for SEU in high-speed SiGe BiCMOS circuits [9]. However, a strictly layout-based variation technique applied to

a bulk SiGe technology has the desirable advantage of being lower in cost compared to process changes (e.g., moving to SOI) for SEU robustness. Additionally, device layout approaches do not incur the increases in circuit area and power consumption common to many circuit hardening techniques. Similar layout-based approaches have been successful in SEU mitigation for CMOS, as demonstrated in [27] and such work for the SiGe HBT clearly warrants further investigation. Although the reductions in Q_C for emitter-center strike will not prevent an upset, the level of suppression of collection from external DT events is quite substantial. Assuming carrier diffusion lengths on the order of 100 μm or more (outside the DT), there is a considerable amount of charge that could potentially be diverted away from the transistor in a broad-beam environment, when there are a substantial number of strikes outside the DT.

Increasing the A_{NR}/A_{DT} ratio is critical in lowering Q_C, and to this end additional structures that increase n-ring width (thereby increasing A_{NR} within the same A_{DT}), while reducing xn_1 would be beneficial. We have demonstrated that in SiGe 8HP, an xn_1 of 2 μm results in an n-ring to collector short, quantifying the limitation of the technique as it applies to internal ring structures. This limitation may be overcome by reductions in the back end of the line (BEOL) thermal cycles and a reduction in the sub-collector doping levels. Another approach may be the combination of process driven hardening techniques (such as the epitaxial Si thickness [25] or SOI [26]), with the layout driven use of the n-ring. Alternatively a buried n-ring, analogous to the triple wells used in CMOS may be considered.

Ultimately, the success of any SiGe RHBD SEE mitigation technique will be determined by the cross-section (σ) versus LET response obtained via broad-beam heavy-ion analysis of actual circuits. The IBICC technique employed in this work gives a good indication, however, of the extent to which layout-based charge collection mitigation is effective, at least for shallow ion strikes. We believe that the ultimate SEU hardening success in SiGe will be achieved via a combination of layout-level RHBD and latch-level RHBD techniques implemented without excessive spatial or temporal redundancy techniques such as TMR. The external n-ring can extended to encompass several minimum spaced devices in a flip-flop or differential pair thereby minimizing the overall area penalty on the circuit level. Compared to TMR, this should yield a 60% reduction in circuit area. The circuit level power penalty will be minimal as the n-ring draws extremely low current (pA) when biased. The technique can also be adapted to mixed signal and analog applications by hardening, the input HBT pair in an operational amplifier for example. Pulsed laser analysis time resoled IBICC techniques could then be used to correlate RHBD charge collection mitigation on the single event transient characteristics.

VI. Summary

Transistor-based layout techniques for mitigating heavy ion triggered charge collection in SiGe HBTs, through the addition of internal and external n-rings, has been presented and validated using ion beam induced charge collection techniques together with 3-D transient ion strike simulations. Up to 90% reduction in collected charge for events outside the DT, and 21% reduction in collected charge for events inside the DT have been demonstrated.

Acknowledgment

The authors would like to thank L. Cohn, K. LaBel, P. Dodd, J. Nance, J.P. Comeau, and the IBM SiGe team for their contributions to this work.

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