The Application of RHBD to n-MOSFETs Intended for Use in Cryogenic-Temperature Radiation Environments

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***Abstract*—Proton and X-ray irradiation effects are investigated in 0.35 μm conventional, annular, and ringed-source radiation-hardening-by-design (RHBD) CMOS devices. Transistors were irradiated with protons at both 300 K and 77 K. Radiation-induced oxide trapped charges in the shallow trench isolation (STI) oxide deplete the p-substrate and effectively shunt the source and drain, inducing off-state leakage. Without the STI, RHBD nFETs exhibit no radiation-induced off-state shunt leakage currents for devices irradiated at both 300 K and 77 K. Conventional 0.35 μm pFETs were not degraded by proton irradiation, since the leakage path cannot be formed in the n-well. A simple CMOS logic inverter shows no degradation in output voltage after proton irradiation for all tested temperature and bias conditions. More advanced 130 nm node nFETs show less TID sensitivity to STI leakage due possibly to the smaller physical STI volume and/or additional doping located on the STI sidewall.**

***Index Terms*—CMOS, cryogenic, cryogenic temperatures, displacement damage, off-state leakage current, radiation hardening by design (RHBD), shallow trench isolation, shallow trench isolation (STI), TID.**

I. Introduction

ELECTRONIC systems deployed in space exploration such as to the Moon and Mars, and even the icy moons of Jupiter often require devices and circuits that are both tolerant to high levels of ionizing radiation and simultaneously reliably operational down to extremely low temperatures (e.g., $+120\,^{\circ}$C to $-230\,^{\circ}$C on the surface of the Moon). To date, only limited data exist for cryogenic irradiation studies of advanced device technologies [1]. Prior work reported the low temperature (77 K) proton response of IBM 5 AM and 8 HP SiGe HBTs [2]. However low-temperature irradiation studies on MOSFETs are necessary to envision extreme environment applications, since SiGe BiCMOS is a preferred platform for mixed-signal circuit design and SiGe technology includes both SiGe HBTs and Si CMOSFETs.

Previous room temperature (300 K) X-ray and proton exposures on unhardened nFET devices from these SiGe BiCMOS technologies show good TID tolerance at both weak and strong channel inversion [3]. However the off-state leakage suffer severely, exhibiting μA-level leakage currents after only a few 100 krad(SiO_2) of ionizing dose. This is clearly a problem for certain circuits. Off-state leakage in nFETs is commonly attributed to radiation-induced oxide trapped charge in the shallow trench isolation (STI) oxide, which can invert the p-substrate in nFETs at the STI edge, thereby creating a shunt leakage path between source and drain, increasing off-state leakage [3]–[9]. An established room temperature radiation-hardening-by-design (RHBD) method to mitigate such off-state leakage is the so-called "enclosed geometry design" [10], [11]. This nFET RHBD approach eliminates STI leakage, and is commonly used for radiation-intense applications, albeit at significant modeling, area, and design overhead. In the present work, we investigate, for the first time, 77 K proton irradiation effects on both conventional n and p-channel and annular n-channel MOSFETs from the IBM 5 AM and 8 HP BiCMOS technologies. The results are compared with those from 63 MeV proton and 10 keV X-ray room temperature irradiation experiments. The 5 AM pFETs and CMOS inverter circuits from 5 AM technology are also tested with 63 MeV protons at 77 K.

II. Device Technology and Experiment

The tested devices include standard layout 3.3 V, 0.35 μm L_{eff} CMOS devices from IBM's first generation, commercial SiGe BiCMOS technology (5 AM), as well as enclosed geometry devices designed for lunar extreme environment applications. Additionally, a third generation SiGe technology with 1.2 V, 130 nm (120 nm on wafer) CMOS devices was also tested to examine the impact of technology scaling on the observed 77 K radiation response. The widths and lengths of the tested devices are listed in Table I.

A schematic cross section of a conventional nFET (identical for both 5 AM and 8 HP), and its equivalent circuit, are illustrated in Fig. 1(a) and (b), respectively. The gate is tied to the substrate via a heavily doped n^+-diffusion area to eliminate plasma-charging effects (this is mandated in the design rules).

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TABLE I
DEVICE DIMENSIONS OF THE 5 AM AND 8 HP DEVICES

Technology	Design	Width	Length
5 AM CMOS (0.35 μ)	Conventional	10 μm	0.35~1.0 μm
	RHBD (Ringed-source)	6.2 μm 24.2 μm	0.5 μm
	RHBD (edgeless annular)	2.0 μm 8.0 μm	0.5 μm
8 HP nFET (0.12 μ)	Conventional	10 μm	0.12μm

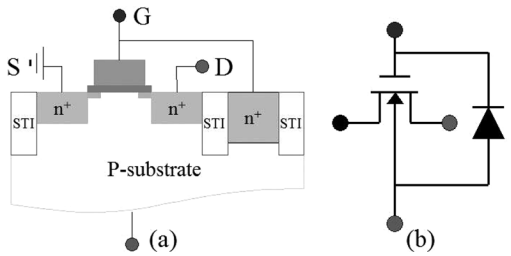

Fig. 1. Schematic cross-sectional diagram of (a) an nFET and (b) its equivalent circuit of the device. The gate is tied to substrate via the n-well, forming a p-n junction. Each device is isolated by shallow trench isolation (STI).

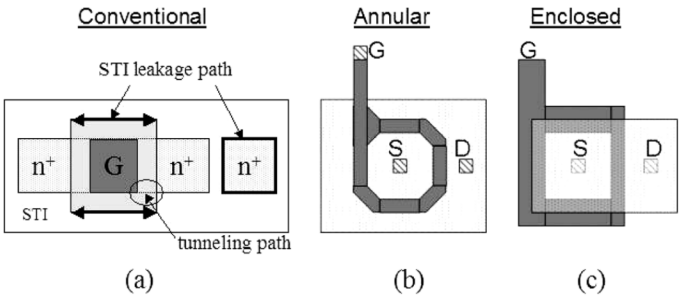

Fig. 2. Schematic top-views of (a) a conventional two-edged, (b) an octagonal annular gate device, and (c) an enclosed ringed-source FETs. The gate-to-substrate diode tie-down is common to all devices.

Fig. 2 shows top views of: (a) the conventional (5 AM, 8 HP) layout, (b) an annular (5 AM) layout, and (c) a ringed source (5 AM) layout, including the parasitic STI leakage path and the potential tunneling path in the gate-drain overlap region.

All devices were wire-bonded into 28-pin DIP packages, followed by 1 hour annealing at 200 °C in an air to remove any moisture. To study ionization effects on 5 AM standard, annular RHBD, and ringed-source devices, 10 keV X-ray irradiation were performed at Vanderbilt University using ARACOR model 4100. Dose rate was 0.54 krad (SiO_2)/s and all irradiations and tests were performed at room temperature in air. 63 MeV proton irradiation tests at both 300 K and low temperatures 77 K were performed at the Crocker Nuclear Laboratory at the University of California at Davis. For the 77 K exposures, packages were mounted on a custom-designed circuit board and dipped directly into a liquid nitrogen-filled polystyrene dewar. The LET of the 63 MeV protons increases by only about 3.9% after traveling through the polystyrene [12]. The sequence of biasing the device during irradiation and then measuring after each dose was performed *in situ* up to a maximum dose of 3 Mrad(SiO_2), at

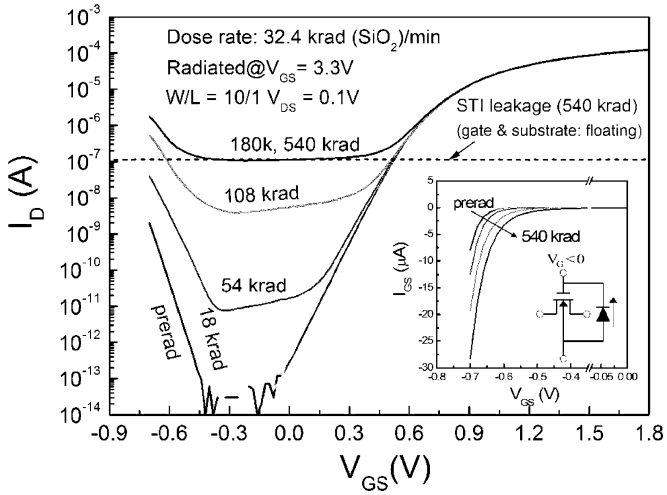

Fig. 3. Off-state I_D–V_{GS} characteristics of a conventional device $(10/1)$ as a function of 10 keV X-ray dose. The inset shows the corresponding gate leakage current as a function of TID at $V_{GS} < 0$.

a dose rate of 1 krad(SiO_2)/s. For the dosimetry measurements, a five-foil secondary emission monitor is used for the calibration against a Faraday cup. Additional 77 K annealing of the devices irradiated at 77 K was performed for 10 hours in the liquid nitrogen dewar, with all pins grounded. Before and after each selected x-ray or proton radiation dose, the current–voltage (I_D–V_{GS}) characteristics were measured using Agilent 4155C semiconductor parameter analyzer.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. X-Ray Irradiation of 5 AM nFETs at 300 K

The room temperature (300 K) 10 keV X-ray irradiation effects on 5 AM conventional and RHBD nFETs are compared in this section. Fig. 3 shows the off-state I_D–V_{GS} characteristics of a conventional device ($W/L = 10$ μm/1.0 μm) irradiated at $V_{GS} = 3.3$ V, for various total doses. The radiation bias condition of $V_{GS} = V_{DD}$ with other terminals grounded is proven to be the worst condition [3]. The increase in the leakage plateau with cumulative TID at $V_{GS} < 0$ is due to damage at the STI to p-substrate interface. The constant dotted line at I_{DS} of 0.1 μA labeled "*STI leakage*" indicates the sole contribution of STI degradation to the drain current, since both the gate and the substrate were floating during the source-drain voltage sweep, with $V_{DS} = 0.1$ V. This constant current meets the plateau where STI leakage current dominates the drain current (-0.6 V $< V_{GS} < 0.2$ V).

The inset figure represents the corresponding gate current variation with dose in the off-state. We attribute this increase to the increasing leakage with total dose of the requisite tie-down diode since oxide and interface traps in the STI around the diode deplete the lightly doped p-substrate, creating a leakage path, which in turn lowers the junction barrier. The independent diode gate-substrate characteristics with other terminals floating verified the gradual leakage current increase with dose. Radiation induced gate current increase in the annular and the ringed-source devices are compatible with that of the standard layout since all three designs have tie down diodes.

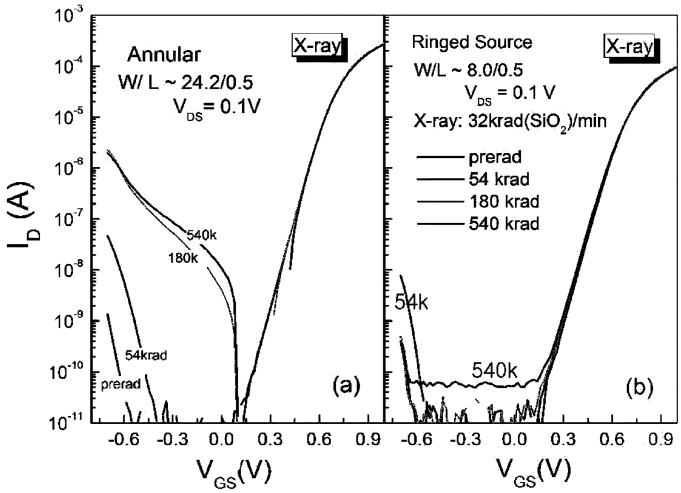

Fig. 4. Off-state I_D–V_{GS} characteristics of: (a) an annular and (b) a ringed-source device as a function of TID. The gate was biased at 3.3 V during irradiation, with all other terminals grounded.

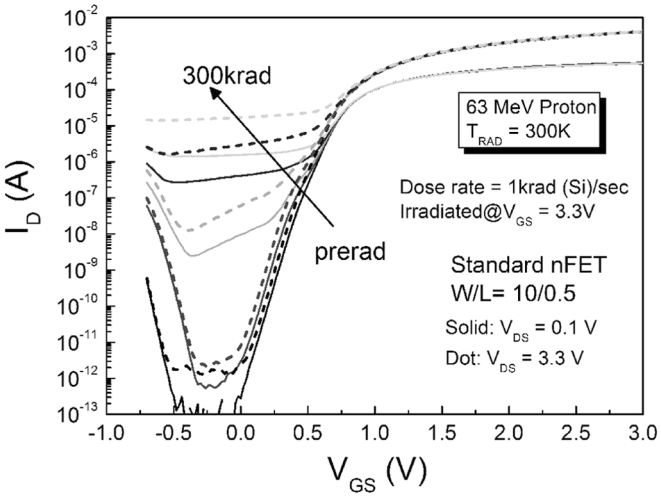

Fig. 5. I_D–V_{GS} characteristics of a conventional device as a function of TID. The gate was biased at 3.3 V during irradiation.

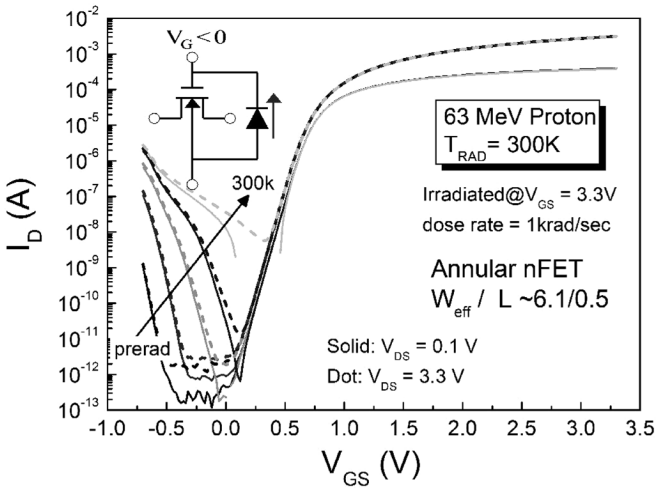

Fig. 6. I_D–V_{GS} characteristics of an annular device as a function of TID. The gate was biased at 3.3 V during irradiation.

The enclosed annular device in Fig. 4(a) shows no current plateau at $V_{GS} < 0$ for the STI-free design shown in the conventional device, but the increase in I_D at $V_{GS} < 0$ is primarily due to the exponential increase in I_G due to the leaky tie-down diode ($|I_G| \sim I_D + I_{SUB}$). For the ringed-source device shown in Fig. 4(b), the gate polysilicon overlaps beyond the active diffusion region, effectively eliminating source-to-drain leakage induced by ionizing radiation. However, the MOS capacitor formed by the ringed-gate is in fact vulnerable to radiation and inverts the substrate easily, as evidenced by the significant increase in the source (recombination) current; after a total dose of 300 krad(SiO_2), $I_{Sub} = 0.19\ \mu$A, $I_D = 3.1$ nA, $I_G = -1.1\ \mu$A, and $I_S = 0.92\ \mu$A, at $V_{GS} = -0.7$ V. Despite the area penalty and extra source current with increasing total dose, the ringed-source layout was found to have the highest TID tolerance of all of the devices under test at 300 K.

B. 63 MeV Proton Irradiation of 5 AM nFETs at 300 K

The room temperature 63 MeV proton irradiation and 90 days of room temperature annealing effects on 5 AM conventional and RHBD nFETs are examined in this section. Fig. 5 shows the I_D–V_{GS} characteristics of a conventional n-FET ($W/L = 10\ \mu$m/0.5 μm) irradiated with 63 MeV protons at 300 K. Again, the off-state leakage current increases with TID due to net positive oxide-trap charge buildup at the STI edge. The magnitude of the STI leakage current depends on the electric field across the S-D region, as evidenced in the higher current for the $V_{DS} = 3.3$ V curve compared to $V_{DS} = 0.1$ V. However, for the proton-irradiated annular device, without STI, the off-state I_D cannot be a function of V_{DS} and the results suggest this phenomenon, as shown in Fig. 6.

A slight stretch-out (~ 50 mV) of the subthreshold characteristics after a total dose of 300 krad(SiO_2), as shown in Fig. 5, is caused by the STI leakage rather than radiation-induced interface traps at Si/SiO_2, since there is no evidence of subthreshold-characteristic change with dose in the RHBD nFETs shown in Fig. 6. Fig. 7(a) and (b) show I_D–V_{GS} characteristics after 90 days of room temperature annealing for the conventional nFET and the RHBD ringed gate nFET, respectively. A considerable amount of radiation-induced oxide-trap charge in the STI region was annealed. The open symbols in Fig. 7 reflect the pure gate current contribution to the off-state drain current, since keeping the substrate floating eliminates gate leakage from the diode. This effectively decouples the contribution of the tie-down diode and the STI leakage impacts on I_D.

Nonetheless, the STI around the tie-down diode becomes susceptible to radiation-induced charge buildup, resulting in an off-state gate current increase, which is reflected as an increase in I_D. Also the increase in gate current with dose is comparable for all of the 5 AM regular and RHBD devices. The drain current decreases in magnitude (at $V_G = -0.7$ V, a pure contribution of the tie-down diode) after room temperature annealing due to the recovery of the degraded diode. A further decrease in off-state I_D occurs when the device is measured with the substrate terminal floating due to the lack of any contribution of diode current (I_G) to I_D. Radiation-induced trap-assisted tunneling across the gate-drain overlap region is often considered a major degradation mechanism in MOSFETs [3]–[9].

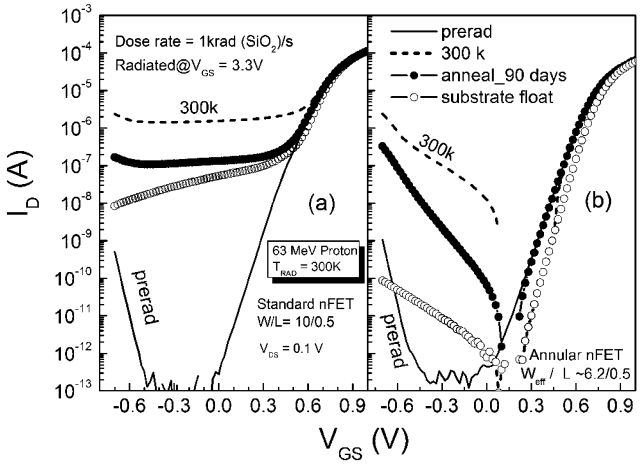

Fig. 7. I_D–V_{GS} characteristics of (a) conventional and (b) annular device after self-annealing at 300 K for 90 days in nitrogen ambient. Open symbols represent the repeated I_D–V_{GS} characteristics with the substrate terminal disconnected.

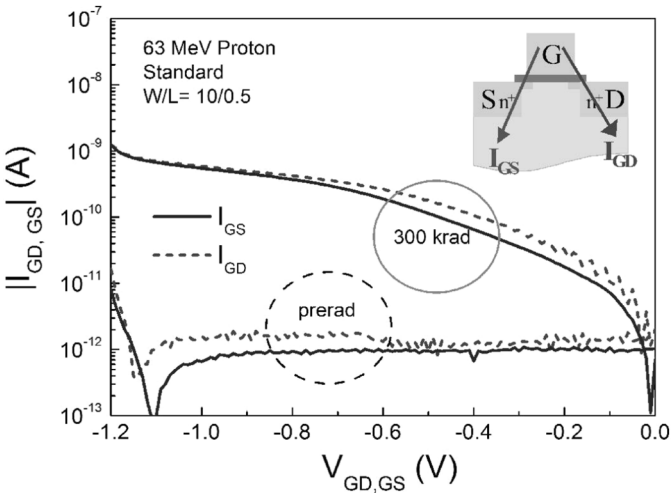

Fig. 8. Gate-drain (source) leakage current characteristics of a conventional device before and after a proton dose of 300 krad. Source (drain) and substrate remain floating during the current sweep. Inset figures show the leakage current paths on device.

The G-D(S) was swept with other terminals floating to extract the pure contribution of the TID induced interface traps at the Si/SiO_2 interface of gate-drain and gate-source overlapped regions on off-state drain current. Fig. 8 shows the gate-to-drain (I_{GD}) and gate-to-source (I_{GS}) currents of the standard device after 300 krad(SiO_2).

We observe an increase in I_{GD} and I_{GS} of approximately two-to-three orders of magnitude as V_{GS} decreases, primarily as a result of radiation-induced trap-assisted tunneling at the G-D edge, as illustrated in the inset figure. It is also worth noting that the STI leakage current contributes more significantly to the total off-state drain leakage relative to the trap-assisted tunneling current, as demonstrated in Fig. 7.

C. Proton Irradiation Effects in 5 AM and 8 HP nFETs at 77 K

The low temperature (77 K) proton irradiation effects on the 5 AM conventional and RHBD nFETs and the more advanced

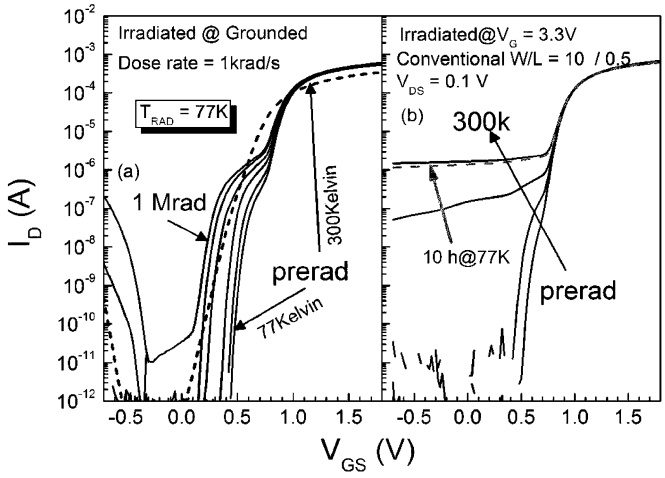

Fig. 9. I_D–V_{GS} characteristics of a conventional device irradiated at 77 K with (a) all pins grounded (0, 30, 100, 300, 600, 1000 krad) and (b) $V_{GS} = 3.3$ V. 10 hrs of annealing was done at 77 K.

node nFETs, 8 HP (0.12 μm node), are introduced in this section. The selected radiation bias conditions are all terminal grounded and $V_{GS} = V_{DD}$ as weak and worst, respectively. Fig. 9(a) and (b) show the I_D–V_{GS} characteristics of a conventional nFET irradiated at 77 K, with all terminals grounded and with $V_{GS} = 3.3$ V, respectively.

The dotted curve in Fig. 9(a) represents a room temperature I_D–V_{GS} characteristic of a pre-rad 5 AM nFET. Note that the low thermal energy of carriers at low gate voltage ($V_G < \sim 0.8$ V, i.e., diffusion-dominated transport) limits the drain leakage current at 77 K. As a result, the threshold voltage increases, but the mobility also increases once channel inversion occurs due to less phonon scattering at the channel at low temperature (i.e., drift dominated transport). For the device grounded during irradiation, the gradual increase of the subthreshold "hump" with total dose is due to the increase of parasitic STI leakage. When the device is irradiated under bias, the amount of leakage current significantly increases, as shown in Fig. 9(b). However, for the annular device, there is no measurable change in the subthreshold characteristics, and in the off-state I_D occurs at V_{GS} down to -0.3 V, for both grounded and biased devices, as shown in Fig. 10(a) and (b). Again, the dotted curve represents the room temperature I_D–V_{GS} characteristics of the annular nFET shown in Fig. 7.

Fig. 11(a) and (b) show the terminal currents of both the standard and annular devices, respectively. All terminal currents were extracted at $V_{GS} = -0.7$ V from devices irradiated at 300 K and 77 K. Note that for the 77 K-irradiated standard device, STI leakage is still the main source of the off-state I_D while there is a no sign of leakage current increase in the edgeless annular device irradiated at 77 K.

The more advanced device, with its thinner gate oxide (8HP MOSFET), shows less TID sensitivity on the STI, and the subthreshold "hump" does not show a significant increase up to 1 Mrad(SiO_2), as shown in Fig. 12. Additional dose up to 3 Mrad(SiO_2) induces increases in I_D via STI leakage as a plateau and through the tie-down diode. We attribute this improved TID tolerance of the 8 HP nFETs to a smaller physical

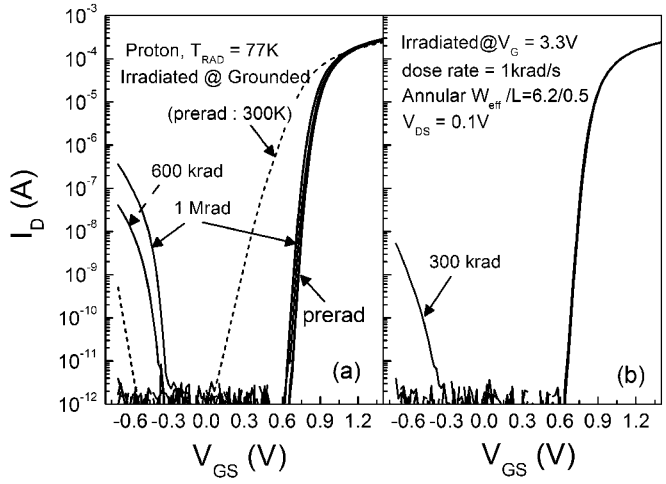

Fig. 10. I_D–V_{GS} characteristics of an annular device irradiated at 77 K with (a) all pins grounded and (b) with V_{GS} at 3.3 V. The exponential increase of I_D at lower V_{GS} (< -0.3 V) is due to the degradation of the tie-down diode.

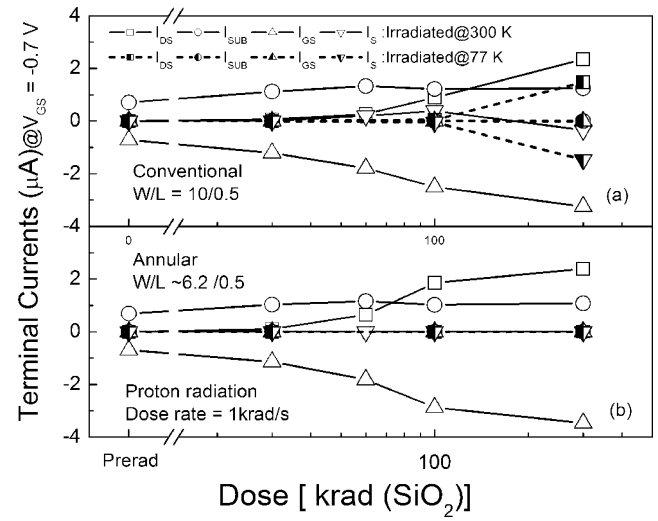

Fig. 11. Each terminal current of (a) a conventional and (b) an annular device versus dose. Devices were irradiated at both 300 K and 77 K, keeping $V_{GS} = 3.3$ V, and other pins grounded. Currents were extracted at $V_{GS} = -0.7$ V.

STI volume, or differences in processing (for example, the final doping profiles may be different along the STI sidewalls).

D. 77 K Proton Irradiation Effects in 5 AM pFETs and CMOS Inverters

Unlike in the nFET, the STI edge in the pFETs is contained within the n-well and no depletion/inversion region can be created by radiation-induced positive charges in the STI, and hence no shunt S/D leakage current can be created along the STI edge. Fig. 13 shows I_D–V_{GS} and the transconductance of proton irradiated pFETs with $W/L = 10/0.35$ at 77 K. There is no change in the off-state I_D–V_{GS} characteristics with proton dose, as expected. The gradual decrease in the peak transconductance with increasing dose is due primarily to channel mobility degradation from the proton-induced displacement damage at the Si/SiO_2 interface and in the n-well. Our previous room temperature 4 MeV proton irradiation study on conventional pFETs confirmed that there is no change in

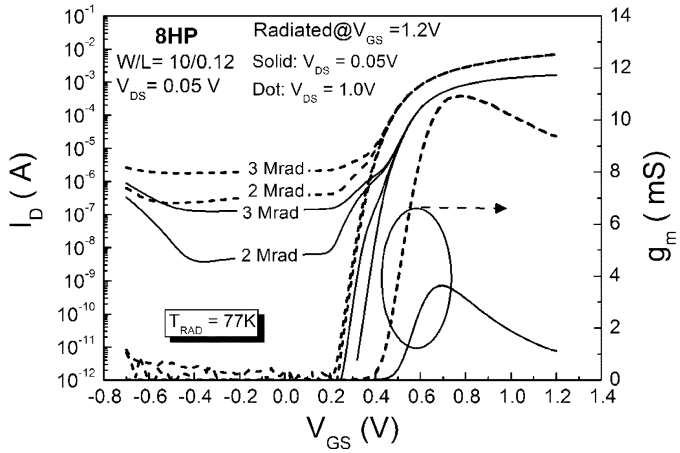

Fig. 12. I_D–V_{GS} characteristics of a conventional 120 nm n-MOSFET irradiated at 77 K. The gate was biased at 1.2 V with all other terminals grounded.

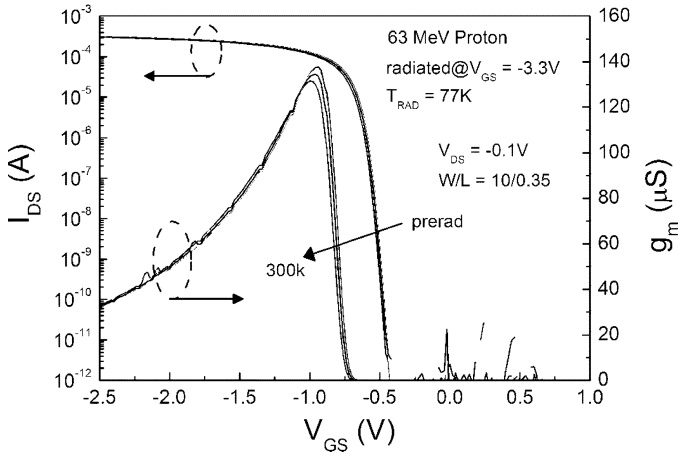

Fig. 13. I_D–V_{GS} and transconductance characteristics of a conventional pFET irradiated at 77 K with $V_{GS} = -3.3$ V.

the off-state characteristics, but a decrease in peak g_m [13]. The negligible degradation observed after 1 Mrad of proton irradiation indicates that conventional pFETs do not require further RHBD for the intended applications.

A simple logic circuit CMOS inverters, which consists of conventional nFETs and pFETs were also tested with 63 MeV protons, at both 300 and 77 K. Fig. 14 shows the input gain voltage versus output drain voltage for an inverter with $W/L = 10/1$, irradiated under bias. The switching voltage increase at 77 K reflects the threshold voltage increase of the nFET at low temperatures. Despite the significant off-state leakage current in the nFET, due to radiation-induced oxide and interface charges in the STI, the switching voltage remains unaffected up to a total dose of 1 Mrad for devices irradiated at both 300 K and 77 K.

IV. Summary

In this work, the TID response of 0.5 μm (5 AM) and 130 nm (8 HP) n-channel MOSFETs, that were designed using different RHBD methods, as a function of irradiation source and temperature is investigated. Standard RHBD techniques are effective in producing TID-robust nFETs for 77 K applications. It is noted that for low-transistor-count analog circuits operating at 77 K,

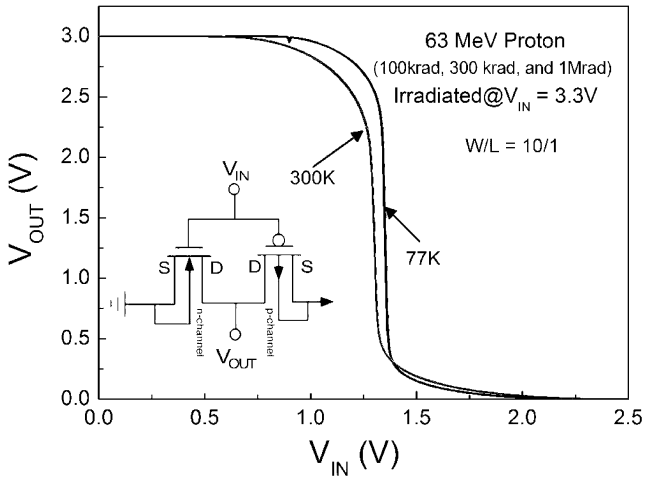

Fig. 14. Output voltage characteristics of an inverter consisted of conventional CMOS devices.

the off-state leakage may be less critical than for high density memory or large logic blocks. The requisite tie-down diodes, with their own (damageable) STI edges, require more effort for improving their TID tolerance at both 300 K and 77 K. Interestingly, however, our findings suggest that migrating to a more aggressive technology node results in superior device-level TID tolerance across temperature, relative to even the most effective RHBD schemes implemented in the older technology node.

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