Government Systems Group

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DATE: August 24, 1995

PPM-95-131

TO: G. Kramer/311
FROM: K. Sahu/300.1 K Sahu
SUBJECT: Radiation Report on 1280A
Control No. 11952

cc: R. Katz/738.2
A. Sharma/311.0
OFA Library/300.1

A radiation evaluation was performed on 1280A (Field Programmable Gate Array) to determine the total dose tolerance of these parts. A brief summary of the test results is provided below. For detailed information, refer to Tables I through V, Figures 1 and 2 and Appendix A.

The total dose testing was performed using a Co^{60} gamma ray source. During the radiation testing, six parts were irradiated under bias (see Table V for bias configuration), and two parts were used as control samples. Three of the irradiated parts (S/N 306, 307 and 308) were burned-in (BI) by the manufacturer before irradiation at 125°C for 160 hours and the other three (S/N 355, 356 and 357) were not burned-in (NBI). This was done in order to determine the effect of burn-in on radiation sensitivity. The wafer number was 9.

The total dose radiation levels were 5, 10, 15 and 20 krads*. The dose rate was between 0.06 and 0.21 krads/hour, depending on the total dose level (see Table II for radiation schedule). After the 20 krad irradiation, parts were annealed at 25°C for 72 hours. Following this, the parts were annealed for an additional 240 hours at 25° for a cumulative total of 312 hours. After each radiation exposure and annealing treatment, parts were electrically tested according to the test conditions and the specification limits** listed in Table III. These tests included six functional tests, three at 1 Mhz, with Vcc = 4.5 V, 5.0 V and 5.5 V, and three at 5 Mhz, with Vcc = 4.5 V, 5.0 V and 5.5 V.

All parts passed initial electrical measurements. All irradiated parts passed all electrical measurements up to and including the 5 krad irradiation.

After the 10 krad irradiation, all ICCL and ICCH measurements exceeded the maximum specification limit of 20 mA, and were above the range (64 mA) of the test equipment.

After the 15 krad irradiation, the range of the test equipment was increased to 256 mA for ICCH and ICCL. All irradiated parts continued to exceed the maximum specification limit for ICCH and ICCL, with readings of approximately 83 to 256 mA. All irradiated parts read within specification limits for all other parameters.

At the 20 krad level, all irradiated parts continued to exceed the maximum specification limit for ICCH and ICCL, with readings of approximately 256 mA, which was at the limit of the range of the test equipment. All irradiated parts read within specification limits for all other parameters.

After annealing for 72 hours and 312 hours at 25°C, no recovery was observed in ICCH and ICCL. All irradiated parts passed all other electrical and functional tests throughout all irradiation and annealing steps.

Table IV provides a summary of the mean and standard deviation values for each parameter after different irradiation exposures and annealing steps.

*The term rads, as used in this document, means rads(silicon). All radiation levels cited are cumulative.
**These are manufacturer's pre-irradiation data specification limits. No post-irradiation limits were provided by the manufacturer at the time these tests were performed.

Readings for ICCL1 and ICCH1 are plotted vs. total dose in Figures. 1 and 2, respectively, for both burned-in (BI) and non burned-in (NBI) parts. As can be seen in both figures, except for one BI part, there does not seem to be a consistent difference between BI and NBI parts.

Any further details about this evaluation can be obtained upon request. If you have any questions, please call me at (301) 731-8954.

TABLE I. Part Information

Generic Part Number:	1280A*
Code 400 Part Number:	1280A
Code 400 Control Number:	11952
Charge Number:	EE44502
Manufacturer:	Actel
Lot Date Code:	unknown
Quantity Tested:	6
Serial Number of Control Samples:	305, 351
Serial Numbers of Radiation Samples:	306, 307, 308 (Burned-In) 355, 356, 357 (not Burned-In)
Wafer No.:	9
Part Function:	Field Programmable Gate Array
Part Technology:	CMOS
Package Style:	84-pin CPGA
Test Equipment:	S-50
Test Engineer:	T. Scharer

* No radiation tolerance/hardness was guaranteed by the manufacturer for this part.

TABLE II. Radiation Schedule for 1280A

EVENTS	DATE
1) INITIAL ELECTRICAL MEASUREMENTS	01/04/95
2) 5 KRAD IRRADIATION (0.12 KRADS/HOUR)	01/10/95
POST-5 KRAD ELECTRICAL MEASUREMENT	01/13/95
3) 10 KRAD IRRADIATION (0.06 KRADS/HOUR)	01/17/95
POST-10 KRAD ELECTRICAL MEASUREMENT	01/20/95
4) 15 KRAD IRRADIATION (0.08 KRADS/HOUR)	01/20/95
POST-15 KRAD ELECTRICAL MEASUREMENT	01/23/95
5) 20 KRAD IRRADIATION (0.21 KRADS/HOUR*)	01/23/95
POST-20 KRAD ELECTRICAL MEASUREMENT	01/24/95
6) 72-HOUR ANNEALING @25°C	01/24/95
POST-72 HOUR ANNEAL ELECTRICAL MEASUREMENT	01/27/95
7) 312-HOUR ANNEALING @25°C	01/27/95
POST-312 HOUR ANNEAL ELECTRICAL MEASUREMENT	02/03/95

PARTS WERE IRRADIATED AND ANNEALED UNDER BIAS; SEE FIGURE 1.

*The dose rate for the 20 krad irradiation was accidentally increased by a factor of approximately 2-3.

Table III. Electrical Characteristics of 1280A

FUNCTIONAL TESTS PERFORMED						
PARAMETER	VCC	VIL	VIH	CONDITIONS	PINS	LIMITS @ -55C,+25C,+125C
FUNCT 1	4.5V	0.0V	4.5V	FREQ=1.000MHZ	ALL I/O	VOL<1.50V , VOH>1.50V
FUNCT 2	5.0V	0.0V	5.0V	FREQ=1.000MHZ	ALL I/O	VOL<1.50V , VOH>1.50V
FUNCT 3	5.5V	0.0V	5.5V	FREQ=1.000MHZ	ALL I/O	VOL<1.50V , VOH>1.50V
FUNCT 4	4.5V	0.0V	4.5V	FREQ=5.000MHZ	ALL I/O	VOL<1.50V , VOH>1.50V
FUNCT 5	5.0V	0.0V	5.0V	FREQ=5.000MHZ	ALL I/O	VOL<1.50V , VOH>1.50V
FUNCT 6	5.5V	0.0V	5.5V	FREQ=5.000MHZ	ALL I/O	VOL<1.50V , VOH>1.50V

DC PARAMETRIC TESTS PERFORMED						
PARAMETER	VCC	VIL	VIH	CONDITIONS	PINS	LIMITS @ -55C,+25C,+125C
VOH1	4.5V	0.00V	4.50V	LOAD=-2.0MA	OUTS	>+2.70V , <+6.50V
VOL1	4.5V	0.00V	4.50V	LOAD=+2.0MA	OUTS	>+0.00V , <+0.40V
IIH	5.5V	0.00V	5.5V	VIN = 5.5V	INS	>-10UA , <+10UA
IIL	5.5V	0.00V	5.5V	VIN = 0.0V	INS	>-10UA , <+10UA
IOSN	5.5V	0.0V	5.5V	VOUT= GND	VCC	>-100MA , <-10MA
ICCL1	4.5V	0.0V	4.5V	VOUT= 0.0V	VCC	>+0.0MA , <+20MA
ICCH1	4.5V	0.0V	4.5V	VOUT= 4.5V	VCC	>+0.0MA , <+20MA
ICCL2	5.0V	0.0V	5.0V	VOUT= 0.0V	VCC	>+0.0MA , <+20MA
ICCH2	5.0V	0.0V	5.0V	VOUT= 5.0V	VCC	>+0.0MA , <+20MA
ICCL3	5.5V	0.0V	5.5V	VOUT= 0.0V	VCC	>+0.0MA , <+20MA
ICCH3	5.5V	0.0V	5.5V	VOUT= 5.5V	VCC	>+0.0MA , <+20MA

AC PARAMETRIC TESTS PERFORMED						
PARAMETER	VCC	VIL	VIH	CONDITIONS	PINS	LIMITS @ -55C,+25C,+125C
TOH	4.5V	0.00V	3.00V	VTEST=2.0V	OUTS	>+0.0NS , <+100NS
TOH	4.5V	0.00V	3.00V	VTEST=2.0V	OUTS	>+0.0NS , <+100NS

Table IV: Total Dose Exposures and Annealing for 1280A /1

Test #	Parameters	Uni	Spec. Lim./2 min	Spec. Lim./2 max	Initials -55°C mean	Initials -55°C sd	Initials 25°C mean	Initials 25°C sd	Initials 125°C mean	Initials 125°C sd	Total DoseExposure (krads) 5 mean	5 sd	10 mean	10 sd	15 mean	15 sd	20/7 mean	20/7 sd	Annealing 72 hrs @25°C mean	72 hrs @25°C sd	Annealing 312 hrs @25°C mean	312 hrs @25°C sd
1	FUNC1, VCC=4.5V, VIL=0.0V, VIH=4.5V, 1MHz				P		P		P		P		P		P		P		P		P	
2	FUNC2, VCC=5.0V, VIL=0.0V, VIH=5.0V, 1MHz				P		P		P		P		P		P		P		P		P	
3.	FUNC3, VCC=5.5V, VIL=0.0V, VIH=5.5V, 1MHz				P		P		P		P		P		P		P		P		P	
4	FUNC4, VCC=4.5V, VIL=0.8V, VIH=4.5V, 5MHz				P		P		P		P		P		P		P		P		P	
5	FUNC5, VCC=5.0V, VIL=0.8V, VIH=5.0V, 5MHz				P		P		P		P		P		P		P		P		P	
6	FUNC6, VCC=5.5V, VIL=0.8V, VIH=5.5V, 5MHz				P		P		P		P		P		P		P		P		P	
7	VOH1	V	3.7	4.5	4.23	.01	4.21	0	4.14	.01	4.21	0	4.21	0	4.19	.01	4.19	.01	4.19	.01	4.19	.01
8	VOL1	mV	0	400	112	4.1	128	5.8	160	25	125	5.5	125	5.5	132	4.9	132	4.1	132	4.1	132	4.1
9	IIH	uA	-10	10	0	0	0	0	0.03	.01	0	0	0	0	0	0	0	0	0	0	0	0
10	IIL	uA	-10	10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	IOSN	mA	-100	-10	-33.8	.43	-31.3	.35	-24.5	.68	-31.1	.90	-31.7	.85	-30.3	.89	-30.0	.35	-30.4	0.5	-30.1	.73
12	ICCL1 /5/6/	mA	0	20	0.13	.03	0.13	.02	0.25	.02	2.25	.40	>64		83.8	3.5	>256		>256		>256	
13	ICCH1 /5/6/	mA	0	20	1.71	.04	1.55	.03	1.37	.03	3.75	.40	>64		89.4	3.4	>256		>256		>256	
14	ICCL2 /5/6/	mA	0	20	0.19	.02	0.18	.02	0.30	.03	3.25	.56	>64		93.1	4.2	>256		>256		>256	
15	ICCH2 /5/6/	mA	0	20	2.09	.05	1.91	.05	1.66	.05	5.22	.64	>64		99.7	4.3	>256		>256		>256	
16	ICCL3 /5/6/	mA	0	20	0.29	.02	0.27	0	0.37	.03	4.42	.69	>64		102	3.9	>256		>256		>256	
17	ICCH3 /5/6/	mA	0	20	2.51	.05	2.25	.05	1.96	.04	6.31	.76	>64		110	4.0	>256		>256		>256	
18	TPLH	ns	0	100	31.5	1.5	30.9	4.7	40.2	8.6	/4		31.0	3.9	34.7	6.0	33.5	6.5	33.6	4.6	35.4	1.4
19	TPHL	ns	0	100	32.8	8.6	29.0	2.8	37.2	4.5	/4		29.5	3.1	33.8	4.7	32.4	3.5	34.4	5.4	33.7	3.3

Notes:

1/ The mean and standard deviation values were calculated over the six parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table.

2/ These are manufacturer's pre-irradiation data sheet specification limits. No post-irradiation limits were provided by the manufacturer at the time the tests were performed.

3/ In the functional Tests, "P" means that all parts passed this test at this irradiation or annealing level, "F" means that all parts failed this test at this irradiation or annealing level and "nPmF" means that n parts passed at this level and m parts failed at this level.

4/ No data were available for this parameter at this irradiation level.

5/ Readings of all parts at the 10 krad irradiation level were beyond the range of the test equipment (64.0mA), therefore the actual values are unknown.

6/ Readings of one part were beyond the range of the test equipment (256 mA) for all six parameters and readings of one part were beyond the range of the test equipment for ICCL2 and ICCH2, therefore, the mean shown here for ICCL2 and ICCH2 is for four samples and the mean for all other ICC parameters is for five samples.

7/ Readings on all parts at the 20 krad level and beyond were beyond the range of the test equipment (256 mA) for all Icc tests, therefore, no mean could be calculated.

Radiation-sensitive parameters: ICCL, ICCH.

Wafer # 9

S/Ns

BI: 306, 307, 308

NBI: 355, 356, 357

control: 305, 351

Table V. Radiation Bias Circuit for 1280A

Signal	Location	Burn-In Board
PRA	C9	VCC
PRB	D7	VCC
MODE	C3	GND
SDI	B14	VCC
SDO	P13	VCC
DCLK	B3	GND
ILIN0	J15	VCC
ILIN1	L1	GND
ILIN2	B6	VCC
ILIN3	H1	GND
ILIN4	R6	VCC
ILIN5	R3	GND
ILIN6	M14	VCC
ILIN7	B2	GND
ILIN8	M1	VCC
ILIN9	F15	GND
ILIN10	C1	VCC
ILIN11	J3	GND
ILIN12	H15	VCC
ILIN13	N2	GND
ILIN14	P9	VCC
ILIN15	N14	GND
ILIN16	C4	VCC
ILIN17	M13	GND
ILIN18	N15	VCC
ILIN19	G3	GND
ILOUT0	L15	VCC/2
ILOUT1	K3	VCC/2
ILOUT2	A6	VCC/2
ILOUT3	J1	VCC/2
ILOUT4	P7	VCC/2
ILOUT5	P3	VCC/2
ILOUT6	P14	VCC/2
ILOUT7	D1	VCC/2
ILOUT8	N1	VCC/2
ILOUT9	G14	VCC/2
ILOUT10	D3	VCC/2
ILOUT11	K1	VCC/2
ILOUT12	G13	VCC/2
ILOUT13	P1	VCC/2
ILOUT14	R10	VCC/2
ILOUT15	L12	VCC/2
ILOUT16	A3	VCC/2
ILOUT17	P15	VCC/2
ILOUT18	R15	VCC/2
ILOUT19	G2	VCC/2

NOTES:

1. VCC = 5.0 V, +/- 0.5 V
2. VCC/2 = 2.5 V +/- 0.25 V
3. All outputs through 2.2 kohm +/- 10% 1/4 W resistors to VCC/2
4. Inputs connected to VCC through 2.2 kohm resistor
5. Inputs connected to GND do not require resistors

VCC: F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5, J14, H2, H14 (NO RESISTOR)

GND: D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6, J13

Table V. Radiation Bias Circuit for 1280A (cont.)

Signal	Location	Burn-In Board
OLIN0	B4	VCC
OLIN1	K15	GND
OLIN2	C7	VCC
OLIN3	E14	GND
OLIN4	C10	VCC
OLIN5	C11	GND
OLIN6	M9	VCC
OLIN7	A10	GND
OLIN8	A11	VCC
OLIN9	D2	GND
OLIN10	L14	VCC
OLIN11	P8	GND
OLIN12	N11	VCC
OLIN13	M3	GND
OLIN14	C5	VCC
OLIN15	F3	GND
OLIN16	C12	VCC
OLIN17	P6	GND
OLIN18	E3	VCC
OLIN19	P11	GND
OLOUT0	A4	VCC/2
OLOUT1	G15	VCC/2
OLOUT2	B7	VCC/2
OLOUT3	E2	VCC/2
OLOUT4	B11	VCC/2
OLOUT5	A12	VCC/2
OLOUT6	N9	VCC/2
OLOUT7	D9	VCC/2
OLOUT8	B10	VCC/2
OLOUT9	A1	VCC/2
OLOUT10	L13	VCC/2
OLOUT11	R7	VCC/2
OLOUT12	R12	VCC/2
OLOUT13	M2	VCC/2
OLOUT14	B5	VCC/2
OLOUT15	F2	VCC/2
OLOUT16	B12	VCC/2
OLOUT17	R5	VCC/2
OLOUT18	B1	VCC/2
OLOUT19	R11	VCC/2
IOGATE	B80	GND
SERIALIN	A7	VCC
SERIALOUT	F1	VCC/2
INX1	R2	VCC
INX2	N5	VCC
IN1A	M15	GND

NOTES:

1. VCC = 5.0 V, +/- 0.5 V
2. VCC/2 = 2.5 V +/- 0.25 V
3. All outputs through 2.2 kohm +/- 10% 1/4 W resistors to VCC/2
4. Inputs connected to VCC through 2.2 kohm resistor
5. Inputs connected to GND do not require resistors

VCC: F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5, J14, H2, H14 (NO RESISTOR)
GND: D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6, J13

Table V. Radiation Bias Circuit for 1280A (cont.)

Signal	Location	Burn-In Board
IN2A	K14	GND
IN_AND3	P12	VCC
IN_AND4	P13	GND
IN_OR3	N6	VCC
IN_OR4	N10	GND
IN_NAND4	M7	VCC
IN_NOR4	N13	GND
DA	L3	VCC
RESET_	P2	GND
ENCNTR	C13	VCC
CNTRLD_	E13	GND
RESETCENTR_	D14	GND
CLOCK	A9	GND
OUTX1	N3	VCC/2
OUTX2	R4	VCC/2
OUTA	K13	VCC/2
O_AND3	R13	VCC/2
O_AND4	N12	VCC/2
O_OR3	P5	VCC/2
O_OR4	P10	VCC/2
O_NAND4	N7	VCC/2
O_NOR4	R14	VCC/2
QA0	L2	VCC/2
QA1	K2	VCC/2
YO11	B13	VCC/2
YO10	E14	VCC/2
YO9	A13	VCC/2
YO8	A15	VCC/2
YO7	D15	VCC/2
YO6	A14	VCC/2
YO5	D13	VCC/2
YO4	C14	VCC/2
YO3	E15	VCC/2
YO2	B15	VCC/2
YO1	C15	VCC/2
YO0	F13	VCC/2

NOTES:

1. VCC = 5.0 V, +/- 0.5 V
2. VCC/2 = 2.5 V +/- 0.25 V
3. All outputs through 2.2 kohm +/- 10% 1/4 W resistors to VCC/2
4. Inputs connected to VCC through 2.2 kohm resistor
5. Inputs connected to GND do not require resistors

VCC: F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5, J14, H2, H14 (NO RESISTOR)
GND: D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6, J13

Figure 1. Comparison of Burned-In (BI) vs. Non Burned-In (NBI) Parts
1280A ICCL Wafer 9

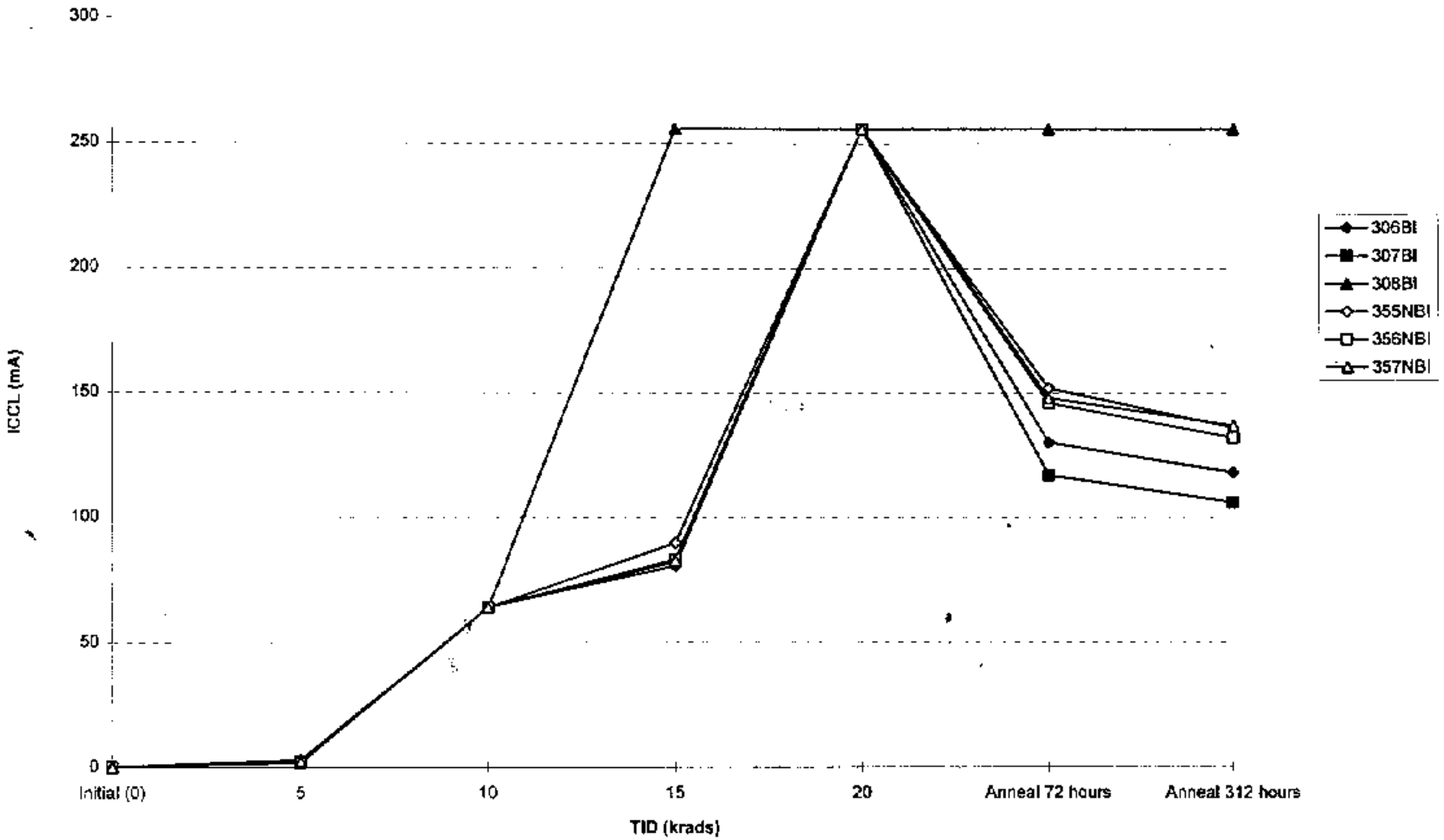
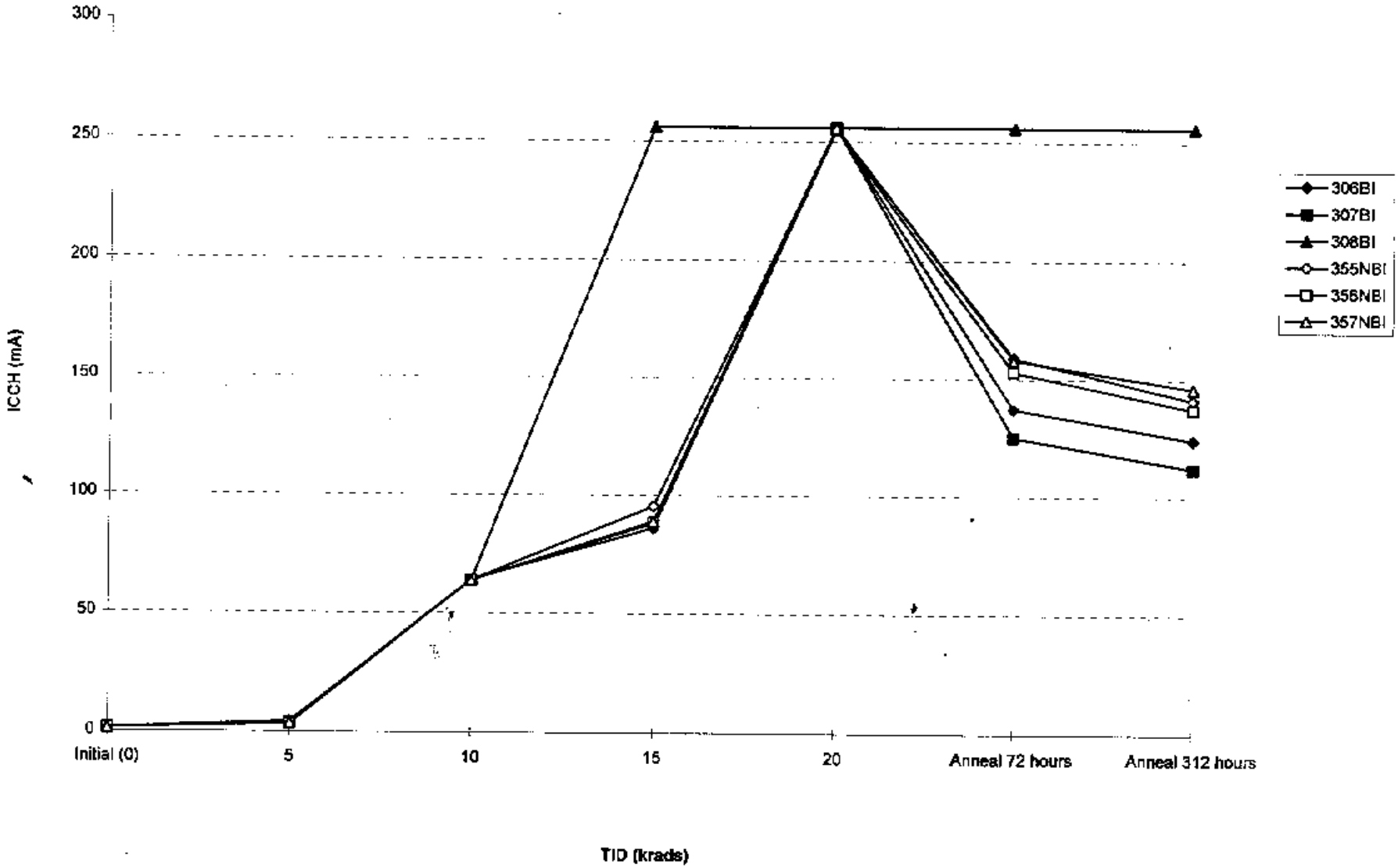


Figure 2. Comparison of Burned-In (BI) vs. Non Burned-In (NBI) Parts
1280A ICCH Wafer 9



Appendix A

Test Chip Pattern

The test chip pattern consists of four sections. The first section tests combinatorial logic, the second tests basic flip-flop characteristics, the third tests the input and output data latches, and the fourth section contains a long shift register and a 12-bit counter with enable, load and reset.

For the gated latches, 20 input and 20 output latches are tested separately. All latches have direct I/O connections, permitting direct control of the data and monitoring of the outputs. Additionally, all latches are operated with a common gate control. This gate is open when the IOGATE signal is a "0" for input latches and a "1" for output latches.

All internal flip-flops are configured a S-Modules. Although flip-flops can be made out of a pair of C-Modules, they are inefficient, particularly when configured in a TMR configuration. Additionally, it is not clear whether future release of Actel tools will continue to support flip-flops made of C-Modules, which have been shown to have a lower susceptibility to SEU's in the 1.2 μm version.

Currently, no C-Module flip-flops are in the design. However, if it is felt that these should be tested during the run, they can be added to the design. Please let me know quickly what you think so the chip design can be finalized.

The internal flip-flops are configured into a shift register consisting of 17 stages of 34 shift flip-flops, all with a common positive edge-triggered clock. The input into the string is on SERIALIN and the output comes from SERIALOUT. The single common clock configuration was chosen to simulate operation in a synchronous device with a heavy clock load to test the clock distribution system. Two inverters are placed within the string to aid in establishing differing biases.

Summary

The circuits in the test chip are simple and based upon a Hughes test. Additions to the original Hughes circuit included logic strings with a variety of gate configurations, and maximum use of the chip by testing a large amount of I/) latches, a long logic string of inverters, and a long string of flip-flops.

Additional material is provided in the following sections for review:

1. TD1280 schematics.
2. TD1280 pin assignments.
3. Logic simulation waveforms and timing diagrams.
4. Static timing analyzer results
    a. Best case
    b/ Worst case
5. Original Hughes test plan.