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UNISYS

DATE: May 20, 1994
TO: A. Sharma/311.2
FROM: K. Sahu/300.1 KS
SUBJECT: Radiation Report on GPEP/PPL
Part No. 1280A
Control No. 8990

PPM-94-012

cc: G. Kramer/311.0
R. Katz/743.0
Library/300.1

A radiation evaluation was performed on 1280A (Gate Array) to determine the total dose tolerance of these parts. A brief summary of the test results is provided below. For detailed information, refer to Tables I through V and Figure 1.

The total dose testing was performed using a cobalt-60 gamma ray source. During the radiation testing, six parts were irradiated under bias (see Table V for bias configuration), and two parts were used as control samples. The total dose radiation levels were 5, 10, 15 and 20 krads*. The dose rate was between 0.05 and 0.11 krads/hour, depending on the total dose level (see Table II for radiation schedule). After the 10 krad irradiation, the parts were annealed for 24 hours at 25°C, 168 hours (cumulative) at 25°C and 336 hours (cumulative) at 25°C, after which the parts were irradiated to 15 krads (cumulative) and 20 krads (cumulative). After the 20 krad irradiation, the parts were annealed for 168 hours at 100°C. After each radiation exposure and annealing step, the parts were electrically tested according to the test conditions and the specification limits** listed in Table III. The electrical tests included three functional tests at 1.0 MHz, with V_{CC} = 4.50 V, 5.00 V and 5.50 V. All parts were programmed with the same test patterns before any radiation testing. The test chip pattern consists of four sections. The first section tests combinatorial logic, the second tests basic flip-flop characteristics, the third tests the input and output data latches, and the fourth section contains a long shift register and a 12-bit counter with enable, load and reset. See Appendix A for more details on test chip patterns.

Initial electrical measurements were performed at three temperatures: -55°C, +25°C and +125°C. All parts passed initial electrical measurements at all three temperatures. All irradiated parts passed all electrical and functional tests up to the 5 krad level. After the 10-krad irradiation, all irradiated parts exceeded the maximum specification limit of 25 mA for both ICCL and ICCH, with readings ranging from 96 to 512 mA. In addition, S/N 5 failed all three functional tests. Three subsequent annealing measurements at25°C were made at 24, 168 and 336 hours. After 24 hours, S/N 5 recovered from functional failure. After the 336-hour annealing period, ICCL and ICCH ranged from 39 to 90 mA. After the 15-krad irradiation, ICCL and ICCH readings increased to between 119 and 512 mA and S/N 5 again failed all three functional tests. After the 20-krad irradiation, All six irradiated parts failed all three functional tests. After annealing for 336 hours at 25°C, all six irradiated parts read within specification limits for all parameters and passed all functional tests. The functional failures of S/N 5 at the 10- and 15-krad level prevented accurate measurement of VOL1, IIH, TPLH and TPHL, and the functional failures of all six irradiated parts at the 20-krad level prevented accurate measurement of VOH1, VOL1, IIH, TPLH and TPHL.

*The term rads, as used in this document, means rads(silicon). All radiation levels cited are cumulative.
**These are manufacturer's non-irradiated data specification limits. No post-irradiation limits were provided by the manufacturer at the time these tests were performed.

After annealing for 168 hours at 100°C, no rebound effects were observed. Table IV provides the mean and standard deviation values for each parameter after different irradiation exposures and annealing steps and Figures 1 and 2 present plots of the values of ICCL and ICCH, respectively, vs. total dose and annealing steps for all six irradiated parts.

Any further details about this evaluation can be obtained upon request. If you have any questions, please call me at (301) 731-8954.

TABLE I. Part Information

Generic Part Number:	1280A
GPEP/PPL Part Number:	1280A
GPEP/PPL Control Number:	8990
Charge Number:	C45256
Manufacturer:	Actel
Lot Date Code:	9328 (S/N 2, 3), 9337 (S/N 1, 4-8)
Quantity Tested:	8
Serial Numbers of Control Samples:	1, 2
Serial Numbers of Radiation Samples:	3, 4, 5, 6, 7, 8
Part Function:	Gate Array
Part Technology:	CMOS, 10 μm
Package Style:	176-pin CPGA
Test Equipment:	S-50
Test Engineer:	A. Karygiannis

* No radiation tolerance/hardness was guaranteed by the manufacturer for this part.

TABLE II. Radiation Schedule for 1280A

EVENTS	DATE
1) INITIAL ELECTRICAL MEASUREMENTS	03/08/94
2) 5 KRAD IRRADIATION (0.11 KRADS/HOUR)	03/08/94
POST-5 KRAD ELECTRICAL MEASUREMENTS	03/10/94
3) 10 KRAD IRRADIATION (0.05 KRADS/HOUR)	03/10/94
POST-10 KRAD ELECTRICAL MEASUREMENTS	03/14/94
4) 24-HOUR ANNEALING @25°C	03/14/94
POST-168 HOUR ANNEAL ELECTRICAL MEASUREMENTS	03/15/94
5) 168-HOUR ANNEALING @25°C	03/14/94
POST-168 HOUR ANNEAL ELECTRICAL MEASUREMENTS	03/21/94
6) 336-HOUR ANNEALING @25°C	03/14/94
POST-336 HOUR ANNEAL ELECTRICAL MEASUREMENTS	03/28/94
7) 15 KRAD IRRADIATION (0.11 KRADS/HOUR)	03/28/94
POST-15 KRAD ELECTRICAL MEASUREMENTS	03/30/94
8) 20 KRAD IRRADIATION (0.11 KRADS/HOUR)	03/30/94
POST-20 KRAD ELECTRICAL MEASUREMENTS	04/01/94
9) 336-HOUR ANNEALING @25°C	04/01/94
POST-336 HOUR ANNEAL ELECTRICAL MEASUREMENTS	04/14/94
10) 168-HOUR ANNEALING @100°C*	04/15/94
POST-168 HOUR ANNEAL ELECTRICAL MEASUREMENTS	04/25/94

*High temperature annealing is performed to accelerate long term time dependent effects (TDE), namely, the "rebound" effect, due to the growth of interface states after the radiation exposure. For more information on the need to perform this test, refer to MIL-STD-8830, Method 1019, Para. 3.10.1.

Table III. Electrical Characteristics of 1280A

FUNCTIONAL TESTS PERFORMED

PARAMETER	VCC	VIL	VIH	CONDITIONS	PINS	LIMITS AT +25C ONLY
FUNCT 1	4.5V	0.0V	4.5V	FREQ=1.000MHz	ALL I/O	VOL<2.25V , VOH>2.25V
FUNCT 2	5.0V	0.0V	5.0V	FREQ=1.000MHz	ALL I/O	VOL<2.50V , VOH>2.50V
FUNCT 3	5.5V	0.0V	5.5V	FREQ=1.000MHz	ALL I/O	VOL<2.75V , VOH>2.75V

DC PARAMETRIC TESTS PERFORMED

PARAMETER	VCC	VIL	VIH	CONDITIONS	PINS	LIMITS @ -55C,+25C,+125C
VOH1	4.5V	0.00V	4.50V	LOAD=-4.0mA	OUTS	>+3.70V , <+4.50V
VOL1	4.5V	0.00V	4.50V	LOAD=+6.0mA	OUTS	>+0.0V , <+0.40V
IIH	5.5V	0.00V	5.5V	VIN = 5.5V	INS	>-10uA , <+10uA
IIL	5.5V	0.00V	5.5V	VIN = 0.0V	INS	>-10uA , <+10uA
IOSN	5.5V	0.0V	5.5V	VOUT= GND	VCC	>-100mA , <+100mA
ICCH	5.5V	0.0V	5.5V	VOUT= 5.5V	VCC	>+0.0UA , <+25mA
ICCL	5.5V	0.0V	5.5V	VOUT= 0.0V	VCC	>+0.0UA , <+25mA

AC PARAMETRIC TESTS PERFORMED

PARAMETER	VCC	VIL	VIH	CONDITIONS	PINS	LIMITS @ -55C,+25C,+125C
TPLH	4.5V	0.00V	3.00V	VTEST=2.0V	OUTS	>+0.0NS , <+100NS
TPHL	4.5V	0.00V	3.00V	VTEST=2.0V	OUTS	>+0.0NS , <+100NS

TABLE IV: Summary of Electrical Measurements after Total Dose Exposures (TDE) and Annealing for 1280A /1

Parameter		Spec. Lim/2 @25°C min	max	Initial @25°C mean	sd	Initial @-55°C mean	sd	Initial @125°C mean	sd	TDE (krads) 5 mean	sd	10* mean	sd	Annealing @25°C 24 hrs		168 hrs		336 hrs	
Func1	Vcc	= 4.5V/3		PASS		PASS		PASS		PASS		5P1F		PASS		PASS		PASS	
Func2	Vcc	= 5.0V/3		PASS		PASS		PASS		PASS		5P1F		PASS		PASS		PASS	
Func3	Vcc	= 5.5V/3		PASS		PASS		PASS		PASS		5P1F		PASS		PASS		PASS	
VOH1	V	3.7	4.5	4.20	.01	4.25	.01	4.14	.01	4.20	.01	3.50	1.6	4.20	.01	4.20	.01	4.20	.01
VOL1	mV	0	400	130	3.2	106	5.6	170	4.2	129	4.6	277	323	131	4.2	131	3.6	131	4.3
IIH	µA	-10	10	0	0	0	0	0.01	.01	0	0	1.6E4	3.7E4	0	0	0	0	0	0
IIL	µA	-10	10	0	0	0	0	-0.02	.22	0	0	-0.02	.01	0	0	0	0	0	0
IOSN	mA	-100	100	-29.1	.60	-34.4	.42	-23.6	.43	-29.3	.62	-23.9	11	-28.8	.60	-29.0	.59	-29.6	.57
ICCL	mA	0	25	2.06	.05	2.44	.03	1.75	.03	12.2	2.6	179	149	103	16	76.2	18	63.5	18
ICCH	mA	0	25	2.04	.05	2.44	.03	1.73	.05	11.7	2.5	178	150	101	17	74.0	19	61.2	19
TPLH	ns	0	100	35.4	4.1	30.8	3.6	42.3	7.4	35.2	3.8	9.1E4	2.9E5	35.2	4.7	35.3	4.3	35.3	4.2
TPHL	ns	0	100	35.0	4.7	30.2	3.0	42.0	5.5	34.6	4.5	2.4E4	1.5E5	35.0	4.5	34.8	4.5	34.8	4.5

Radiation-sensitive parameters were VOL1, IIH, IIL, ICCL, ICCH, TPLH and TPHL.

1/ The mean and standard deviation values were calculated over the six parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table.

2/ These are manufacturers' non-irradiated data sheet specification limits. No post-irradiation limits were provided by the manufacturer at the time the tests were performed.

3/ "PASS" means that all irradiated parts passed this functional test at this irradiation or annealing level. "FAIL" means that all irradiated parts failed this test at this irradiation or annealing level. "nPmF" means that n parts passed and m parts failed the test at this level.

* At the 10 krad and 15 krad irradiation levels, one part failed functionally and was out of specification limits for most other parameters. All other irradiated parts continued to read within specification limits for all parameters.

** AC measurements were not performed at this level due to equipment problems.

TABLE IV: Summary of Electrical Measurements after Total Dose Exposures (TDE) and Annealing for 1280A /1

Parameter		Spec. Lim/2 @25°C min	max	TDE (krads) 15* mean	sd	20 mean	sd	Annealing 336 hrs @25°C mean	sd	168 hrs @100°C mean	sd
Func1	Vcc = 4.5V/3			5P1F		FAIL		PASS		PASS	
Func2	Vcc = 5.0V/3			5P1F		FAIL		PASS		PASS	
Func3	Vcc = 5.5V/3			5P1F		FAIL		PASS		PASS	
VOH1	V	3.7	4.5	3.49	1.6	Fail		4.19	.01	4.19	7.7
VOL1	mV	0	400	279	319	Fail		134	5.5	131	4.0
IIH	µA	-10	10	6270	1.4E4	5.7E4	1.7E4	0	0	0	0
IIL	µA	-10	10	0	0	-0.04	.03	0	0	0	0
IOSN	mA	-100	100	-23.6	11	0	0	-28.5	.56	-28.6	.65
ICCL	mA	0	25	219	132	501	26	131	31	5.63	1.5
ICCH	mA	0	25	217	134	147	371	130	16	7.53	1.5
TPLH	ns	0	100	1.1E5	1.1E5	4.4E5	5.0E5	**		15.3	5.3
TPHL	ns	0	100	9.5E4	2.9E5	3.0E5	4.9E5	**		15.6	5.0

Radiation-sensitive parameters were VOL1, IIH, IIL, ICCL, ICCH, TPLH and TPHL.

1/ The mean and standard deviation values were calculated over the six parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table.

2/ These are manufacturers' non-irradiated data sheet specification limits. No post-irradiation limits were provided by the manufacturer at the time the tests were performed.

3/ "PASS" means that all irradiated parts passed this functional test at this irradiation or annealing level. "FAIL" means that all irradiated parts failed this test at this irradiation or annealing level. "nPmF" means that n parts passed and m parts failed the test at this level.

* At the 10 krad and 15 krad irradiation levels, one part failed functionally and was out of specification limits for most other parameters. All other irradiated parts continued to read within specification limits for all parameters.

**AC measurements were not performed at this level due to equipment problems.

Table V. Radiation Bias Circuit for 1280A

Signal	Location	Burn-In Board
PRA	C9	VCC
PRB	D7	VCC
MODE	C3	GND
SDI	B14	VCC
SDO	P13	VCC
DCLK	B3	GND
ILINO	J15	VCC
ILIN1	L1	GND
ILIN2	B6	VCC
ILIN3	H1	GND
ILIN4	R6	VCC
ILIN5	R3	GND
ILIN6	M14	VCC
ILIN7	B2	GND
ILIN8	M1	VCC
ILIN9	F15	GND
ILIN10	C1	VCC
ILIN11	J3	GND
ILIN12	H15	VCC
ILIN13	N2	GND
ILIN14	P9	VCC
ILIN15	N14	GND
ILIN16	C4	VCC
ILIN17	M13	GND
ILIN18	N15	VCC
ILIN19	G3	GND
ILOUT0	L15	VCC/2
ILOUT1	K3	VCC/2
ILOUT2	A6	VCC/2
ILOUT3	J1	VCC/2
ILOUT4	P7	VCC/2
ILOUT5	P3	VCC/2
ILOUT6	P14	VCC/2
ILOUT7	D1	VCC/2
ILOUT8	N1	VCC/2
ILOUT9	G14	VCC/2
ILOUT10	D3	VCC/2
ILOUT11	K1	VCC/2
ILOUT12	G13	VCC/2
ILOUT13	P1	VCC/2
ILOUT14	R10	VCC/2
ILOUT15	L12	VCC/2
ILOUT16	A3	VCC/2
ILOUT17	P15	VCC/2
ILOUT18	R15	VCC/2
ILOUT19	G2	VCC/2

NOTES:

1. VCC = 5.0 V, +/- 0.5 V
2. VCC/2 = 2.5 V +/- 0.25 V
3. All outputs through 2.2 kohm +/- 10% 1/4 W resistors to VCC/2
4. Inputs connected to VCC through 2.2 kohm resistor
5. Inputs connected to GND do not require resistors

VCC: F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5, J14, H2, H14 (NO RESISTOR)

GND: D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6, J13

Table V. Radiation Bias Circuit for 1280A (cont.)

Signal	Location	Burn-In Board
OLIN0	B4	VCC
OLIN1	K15	GND
OLIN2	C7	VCC
OLIN3	E14	GND
OLIN4	C10	VCC
OLIN5	C11	GND
OLIN6	M9	VCC
OLIN7	A10	GND
OLIN8	A11	VCC
OLIN9	D2	GND
OLIN10	L14	VCC
OLIN11	P8	GND
OLIN12	N11	VCC
OLIN13	M3	GND
OLIN14	C5	VCC
OLIN15	F3	GND
OLIN16	C12	VCC
OLIN17	P6	GND
OLIN18	E3	VCC
OLIN19	P11	GND
OLOUT0	A4	VCC/2
OLOUT1	G15	VCC/2
OLOUT2	B7	VCC/2
OLOUT3	E2	VCC/2
OLOUT4	B11	VCC/2
OLOUT5	A12	VCC/2
OLOUT6	N9	VCC/2
OLOUT7	D9	VCC/2
OLOUT8	B10	VCC/2
OLOUT9	A1	VCC/2
OLOUT10	L13	VCC/2
OLOUT11	R7	VCC/2
OLOUT12	R12	VCC/2
OLOUT13	M2	VCC/2
OLOUT14	B5	VCC/2
OLOUT15	F2	VCC/2
OLOUT16	B12	VCC/2
OLOUT17	R5	VCC/2
OLOUT18	B1	VCC/2
OLOUT19	R11	VCC/2
IOGATE	B80	GND
SERIALIN	A7	VCC
SERIALOUT	F1	VCC/2
INX1	R2	VCC
INX2	N5	VCC
IN1A	M15	GND

NOTES:

1. VCC = 5.0 V, +/- 0.5 V
2. VCC/2 = 2.5 V +/- 0.25 V
3. All outputs through 2.2 kohm +/- 10% 1/4 W resistors to VCC/2
4. Inputs connected to VCC through 2.2 kohm resistor
5. Inputs connected to GND do not require resistors

VCC: F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5, J14, H2, H14 (NO RESISTOR)

GND: D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6, J13

Table V. Radiation Bias Circuit for 1280A (cont.)

Signal	Location	Burn-In Board
IN2A	K14	GND
IN_AND3	P12	VCC
IN_AND4	P13	GND
IN_OR3	N6	VCC
IN_OR4	N10	GND
IN_NAND4	M7	VCC
IN_NOR4	N13	GND
DA	L3	VCC
RESET_	P2	GND
ENCNTR	C13	VCC
CNTRLD_	E13	GND
RESETCENTR_	D14	GND
CLOCK	A9	GND
OUTX1 *	N3	VCC/2
OUTX2	R4	VCC/2
OUTA	K13	VCC/2
O_AND3	R13	VCC/2
O_AND4	N12	VCC/2
O_OR3	P5	VCC/2
O_OR4	P10	VCC/2
O_NAND4	N7	VCC/2
O_NOR4	R14	VCC/2
QA0	L2	VCC/2
QA1	K2	VCC/2
YO11	B13	VCC/2
YO10	E14	VCC/2
YO9	A13	VCC/2
YO8	A15	VCC/2
YO7	D15	VCC/2
YO6	A14	VCC/2
YO5	D13	VCC/2
YO4	C14	VCC/2
YO3	E15	VCC/2
YO2	B15	VCC/2
YO1	C15	VCC/2
YO0	F13	VCC/2

NOTES:

1. VCC = 5.0 V, +/- 0.5 V
2. VCC/2 = 2.5 V +/- 0.25 V
3. All outputs through 2.2 kohm +/- 10% 1/4 W resistors to VCC/2
4. Inputs connected to VCC through 2.2 kohm resistor
5. Inputs connected to GND do not require resistors

VCC: F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5, J14, H2, H14 (NO RESISTOR)

GND: D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6, J13

Figure 1. ICCL vs. Total Dose & Annealing Time for 1280A

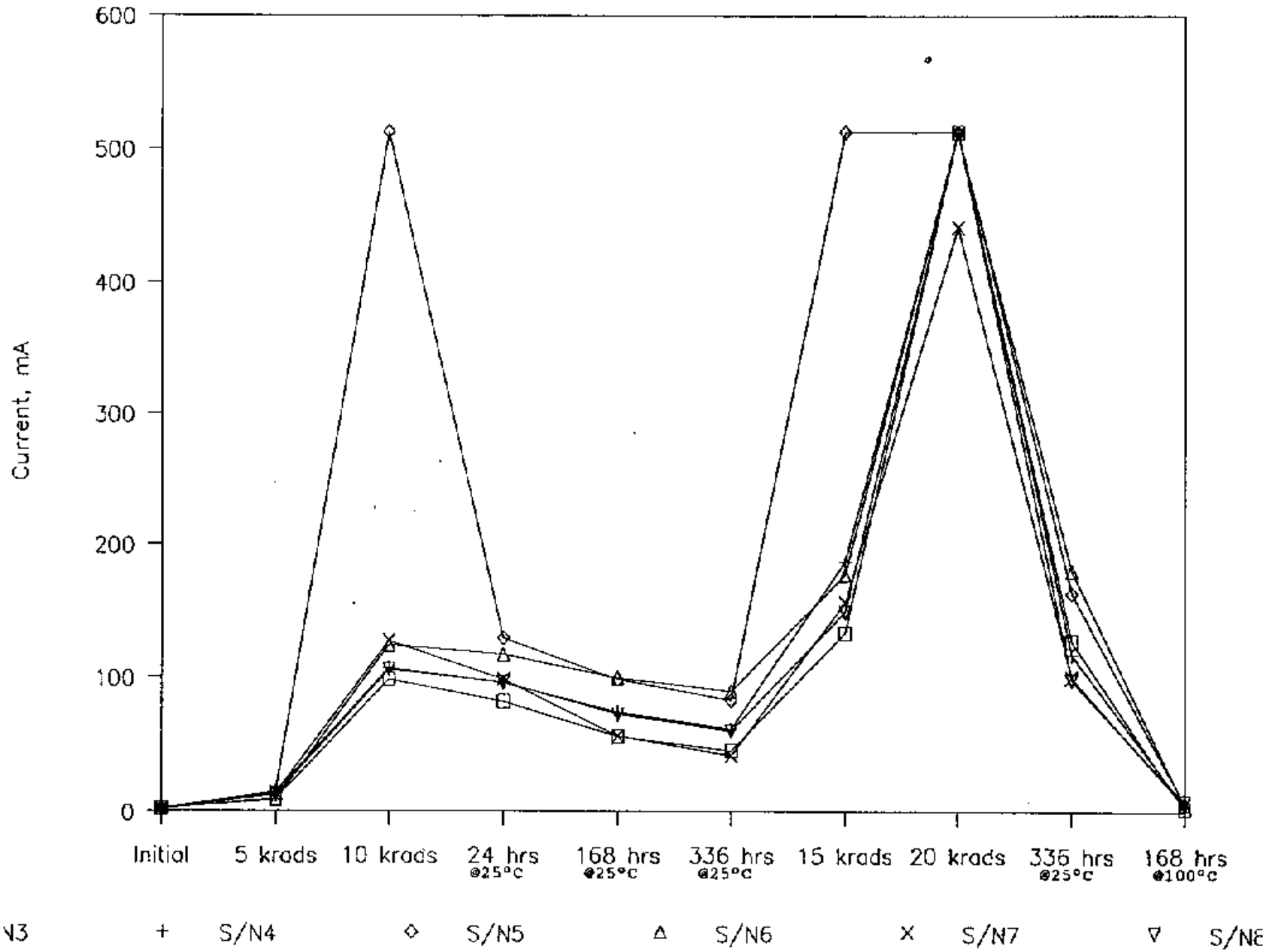
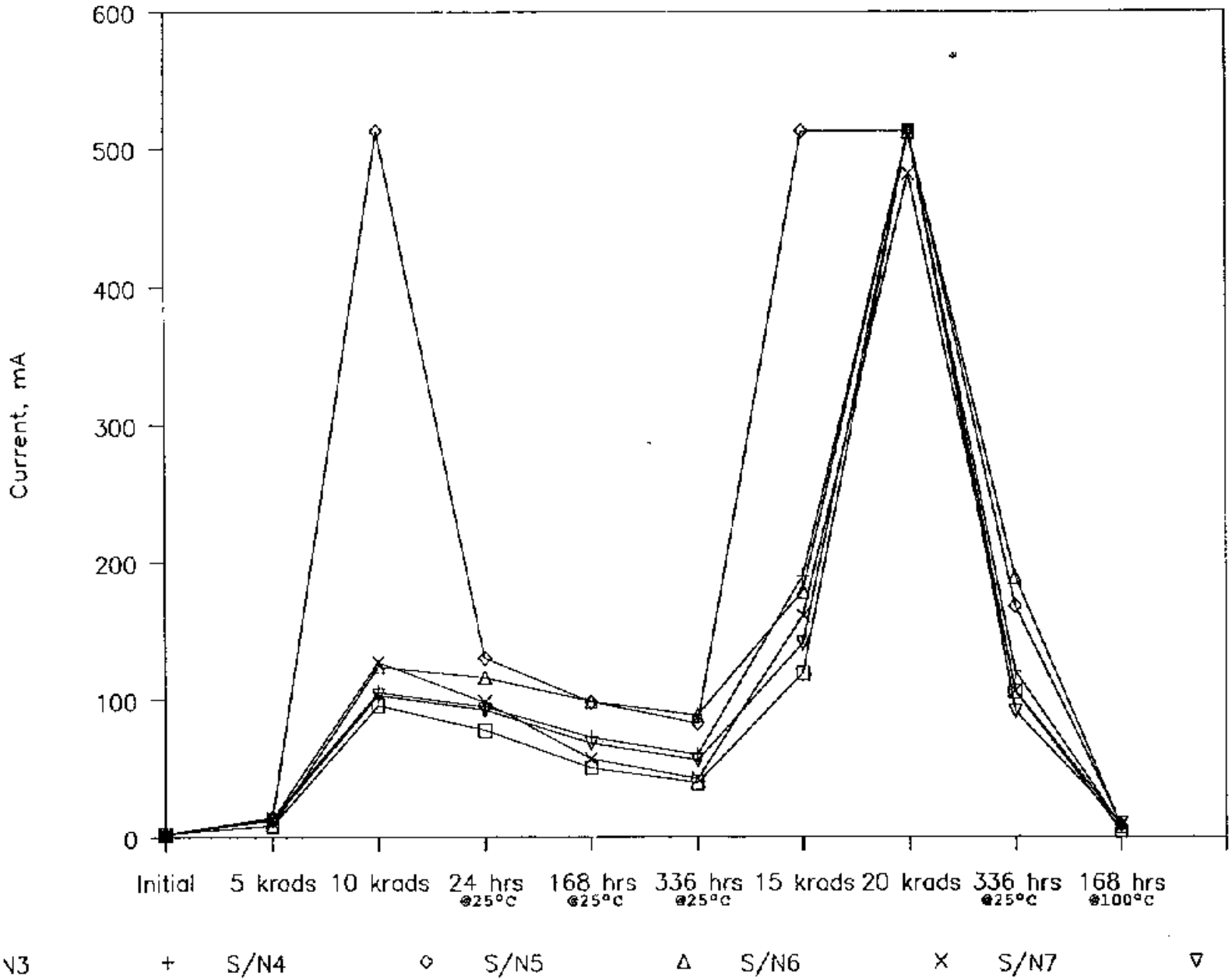


Figure 2. ICCH vs. Total Dose & Annealing Time for 1280A



Appendix A

Test Chip Pattern

The test chip pattern consists of four sections. The first section tests combinatorial logic, the second tests basic flip-flop characteristics, the third tests the input and output data latches, and the fourth section contains a long shift register and a 12-bit counter with enable, load and reset.

For the gated latches, 20 input and 20 output latches are tested separately. All latches have direct I/O connections, permitting direct control of the data and monitoring of the outputs. Additionally, all latches are operated with a common gate control. This gate is open when the IOGATE signal is a "0" for input latches and a "1" for output latches.

All internal flip-flops are configured a S-Modules. Although flip-flops can be made out of a pair of C-Modules, they are inefficient, particularly when configured in a TMR configuration. Additionally, it is not clear whether future release of Actel tools will continue to support flip-flops made of C-Modules, which have been shown to have a lower susceptibility to SEU's in the 1.2 μm version.

Currently, no C-Module flip-flops are in the design. However, if it is felt that these should be tested during the run, they can be added to the design. Please let me know quickly what you think so the chip design can be finalized.

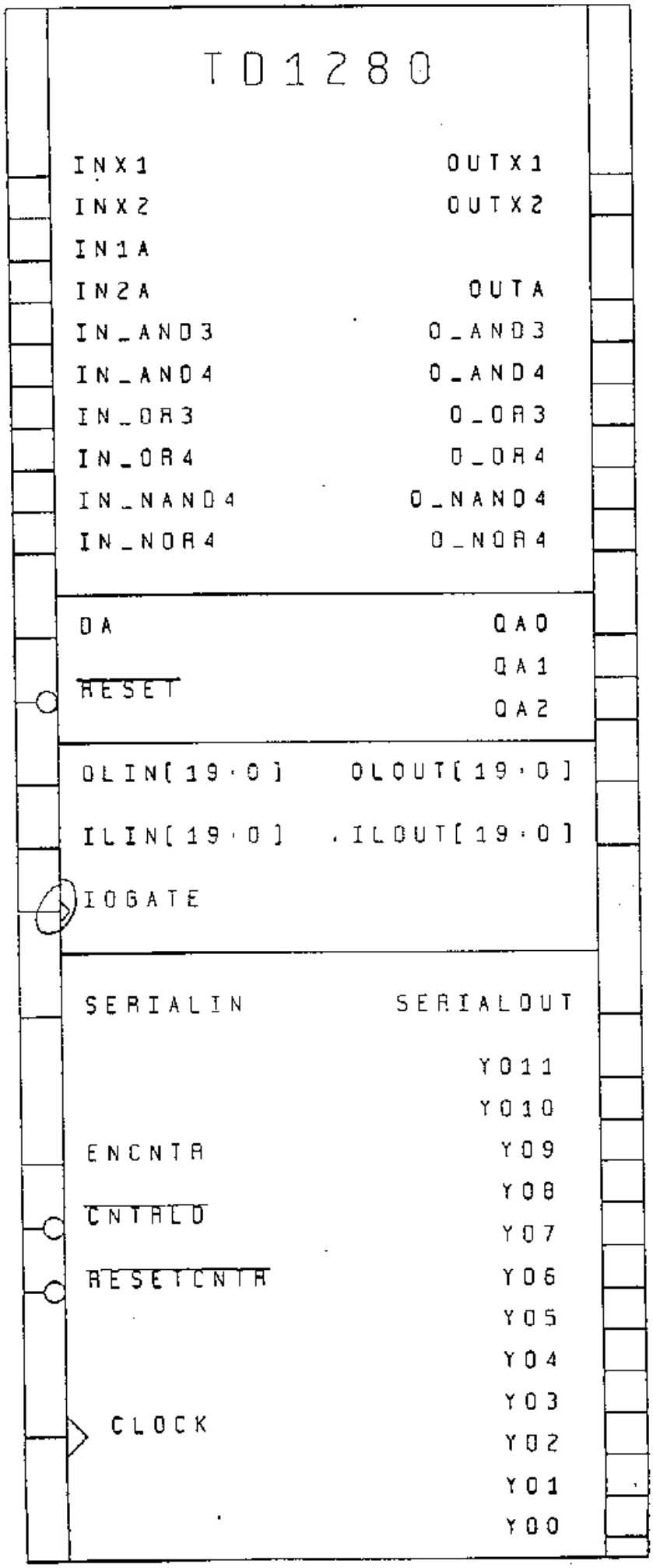
The internal flip-flops are configured into a shift register consisting of 17 stages of 34 shift flip-flops, all with a common positive edge-triggered clock. The input into the string is on SERIALIN and the output comes from SERIALOUT. The single common clock configuration was chosen to simulate operation in a synchronous device with a heavy clock load to test the clock distribution system. Two inverters are placed within the string to aid in establishing differing biases.

Summary

The circuits in the test chip are simple and based upon a Hughes test. Additions to the original Hughes circuit included logic strings with a variety of gate configurations, and maximum use of the chip by testing a large amount of I/) latches, a long logic string of inverters, and a long string of flip-flops.

Additional material is provided in the following sections for review:

1. TD1280 schematics.
2. TD1280 pin assignments.
3. Logic simulation waveforms and timing diagrams.
4. Static timing analyzer results
    a. Best case
    b/ Worst case
5. Original Hughes test plan.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INX2
IN1A
IN2A
IN_AND3
IN_AND4
IN_OR3
IN_OR4
IN_NAND4
IN_NOR4
OUTX1
OUTX2
OUTA
O_AND3
O_AND4
O_OR3
O_OR4
O_NAND4
O_NOR4
DA
RESET
QA0
QA1
QA2
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ENCNTR
CNTRLD
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Y05
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Y03
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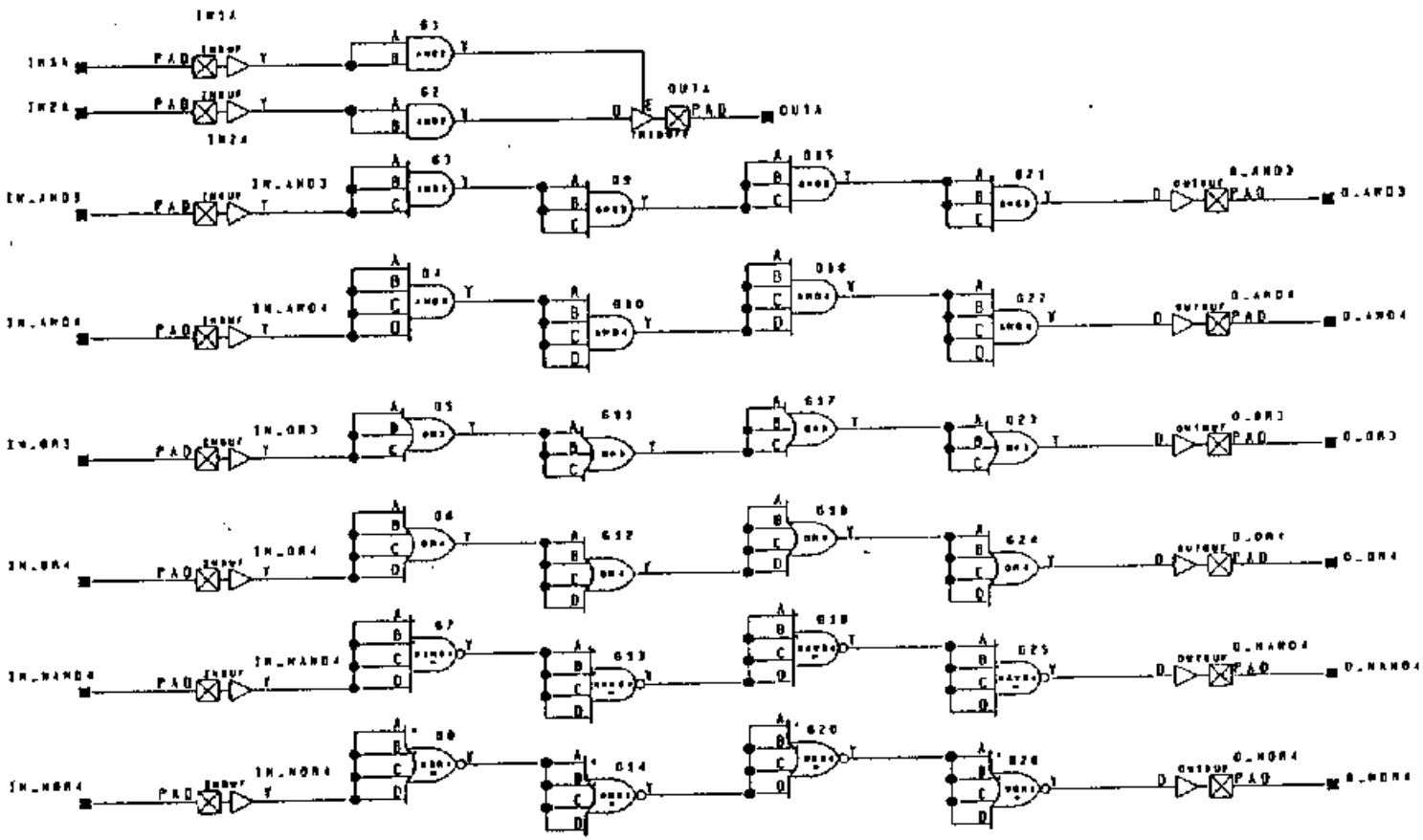

VIEWlogic

TO1280.1

ACTEL 1280 TOTAL DOSE CKT

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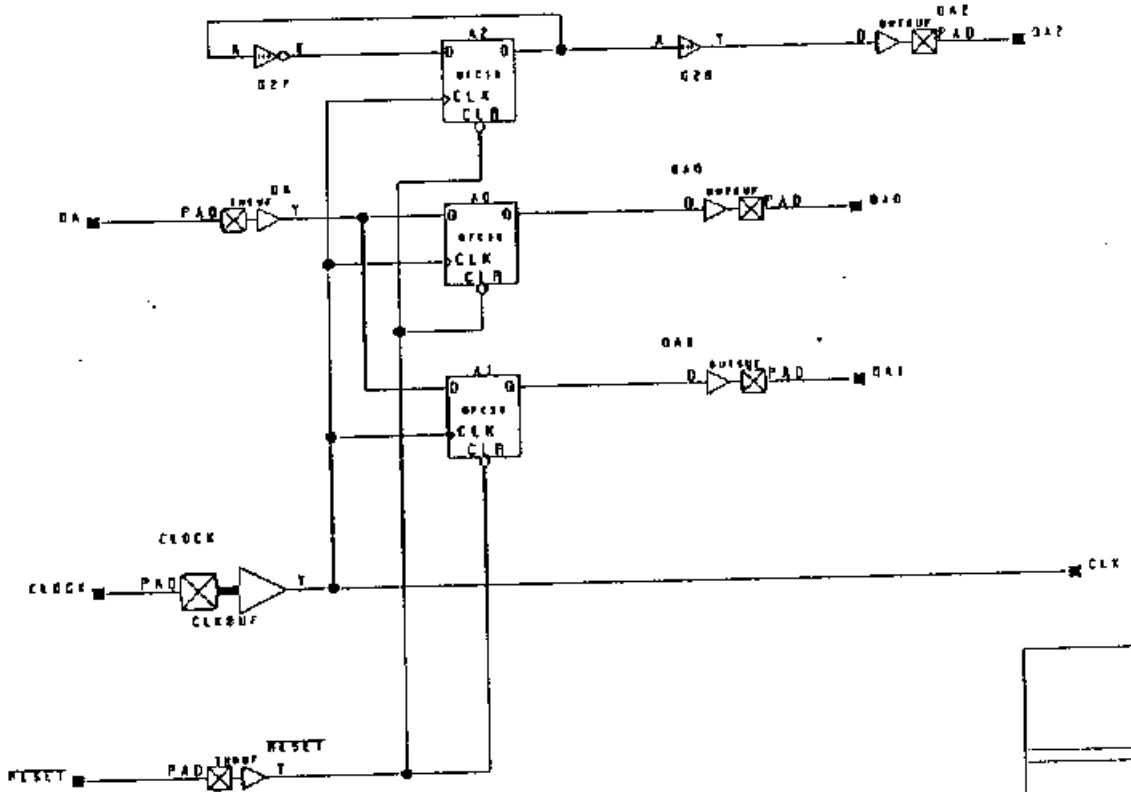

VIEWlogic

T01280.2

ACIEL 1280 TOTAL DOSE CKT

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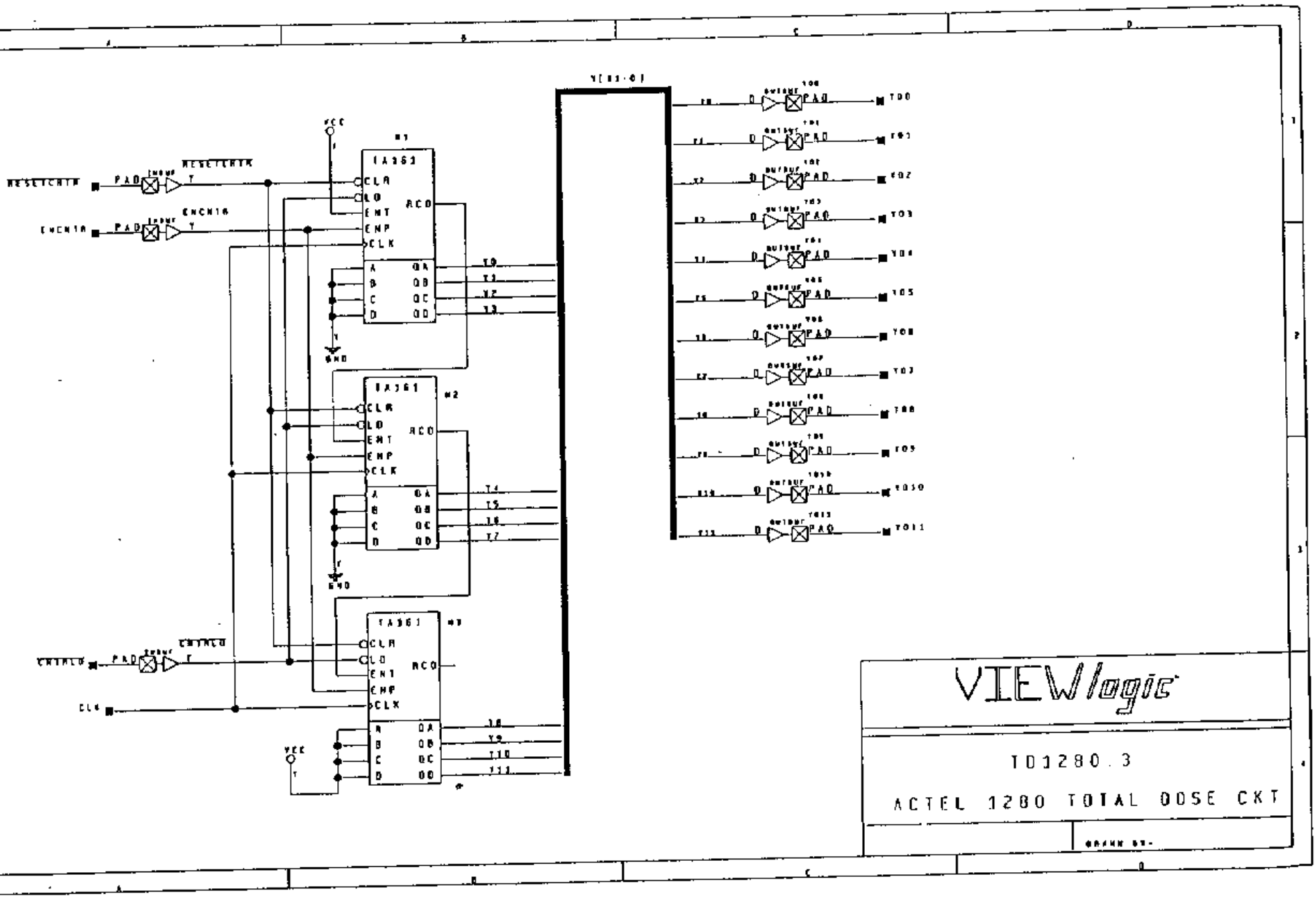
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ENCNTR
CNTRLD
CLK
VCC
GND
TA361
CLR
LD
ENT
ENP
CLK
RCO
A
B
C
D
QA
QB
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TD2
TD3
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TD5
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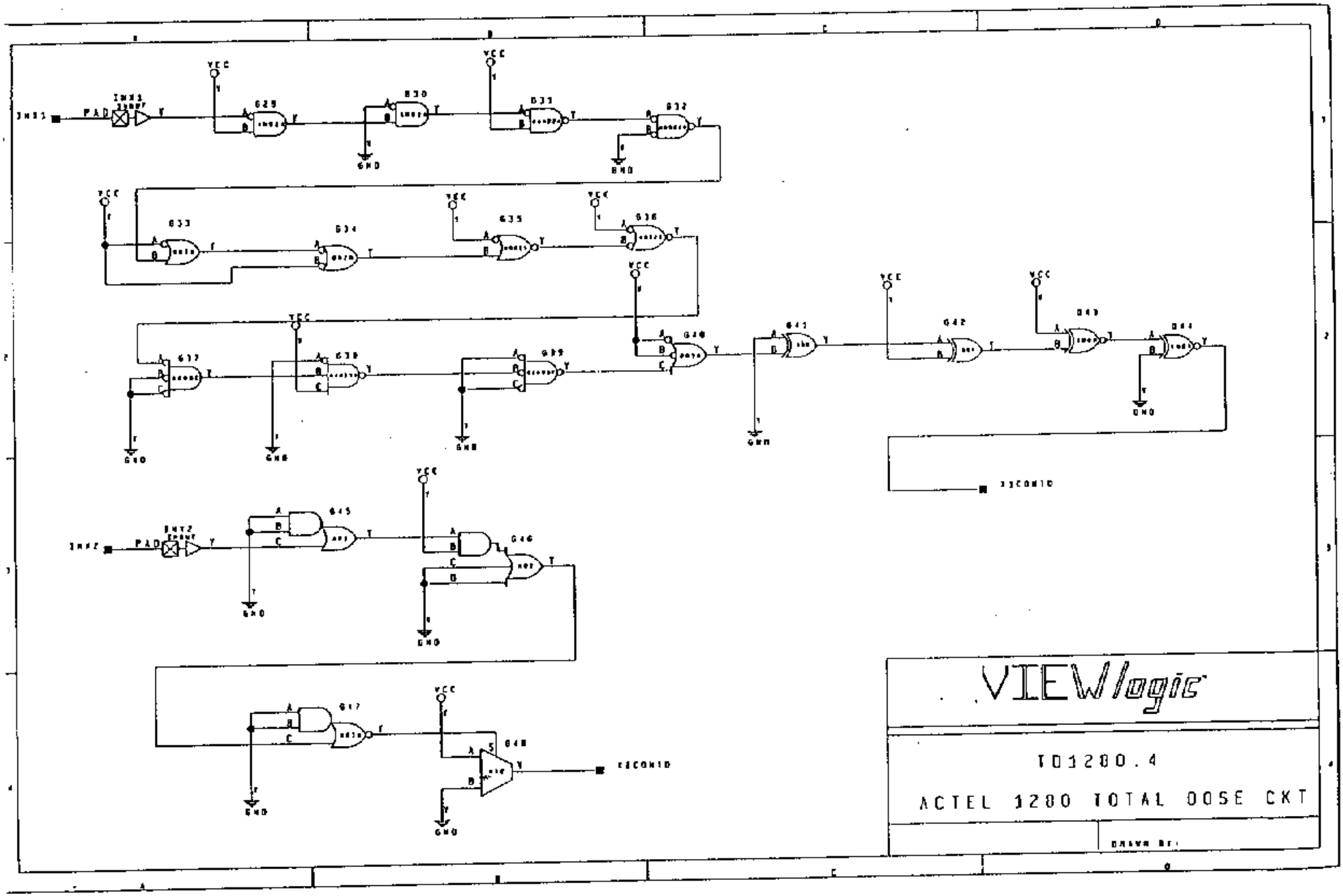
TD11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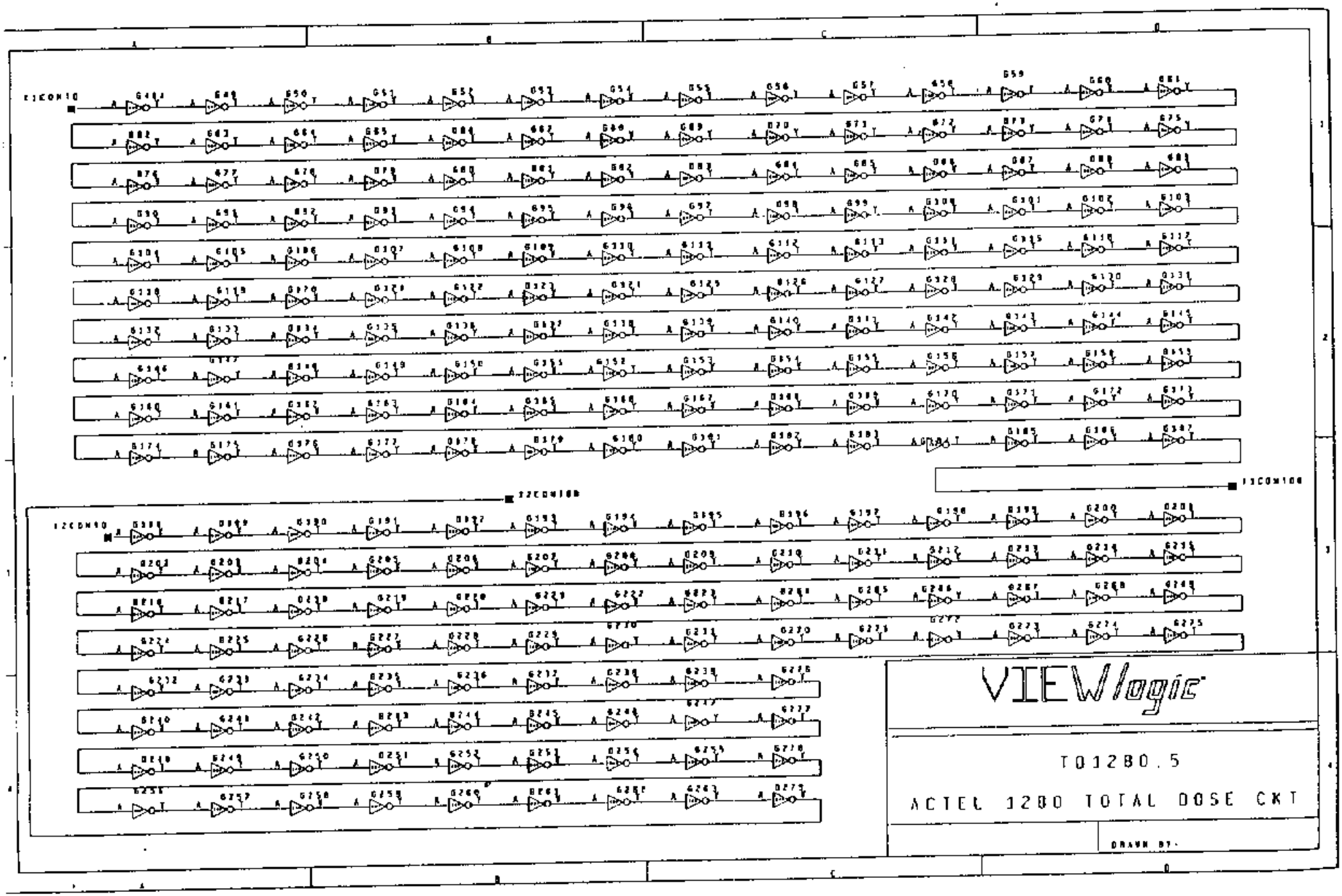
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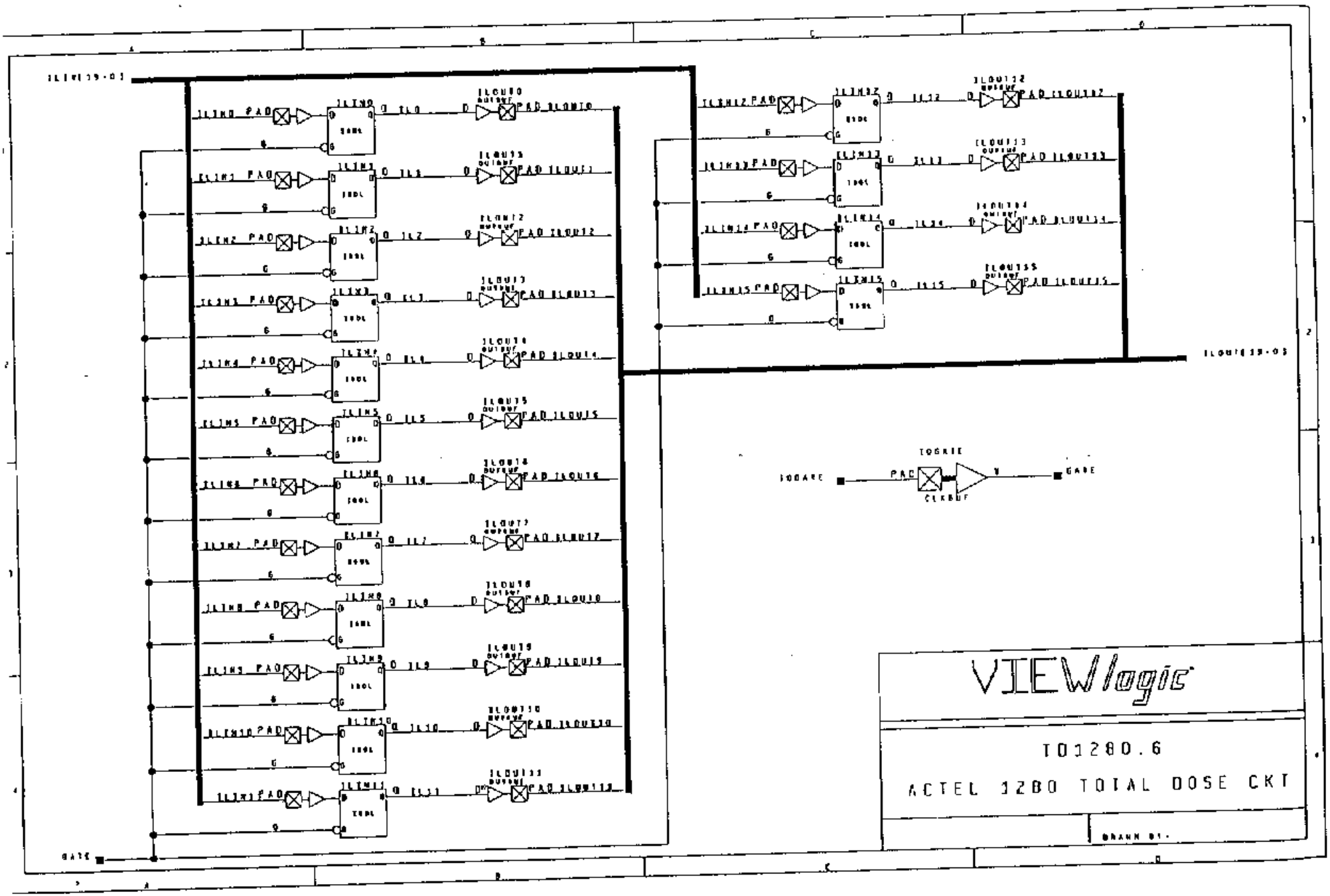
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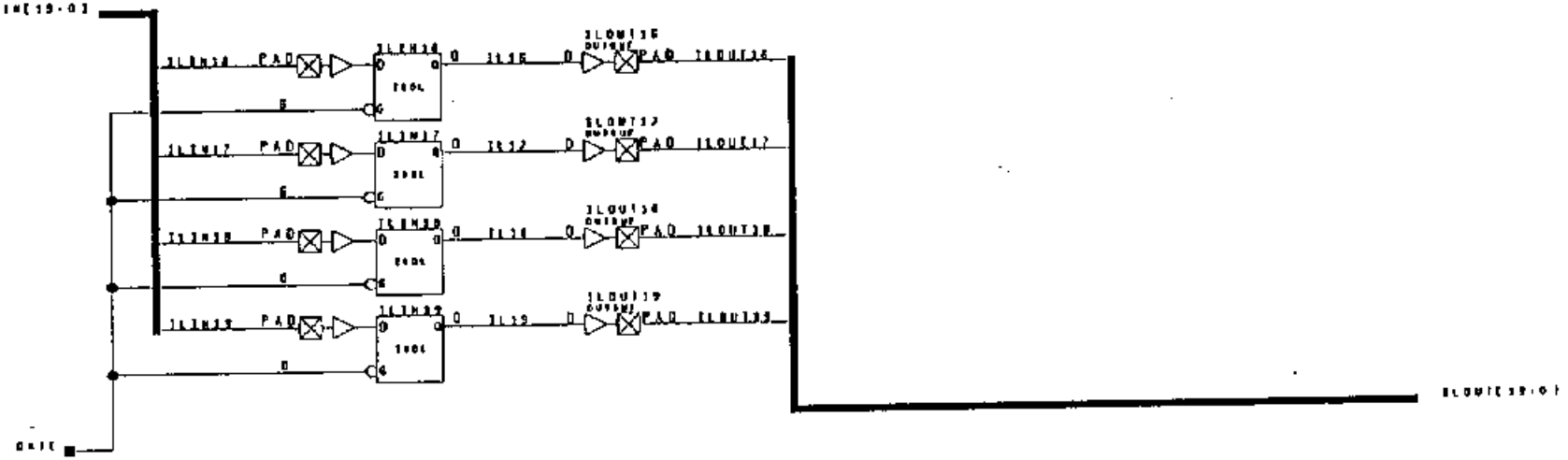

VIEWlogic

TD1280.7

ACTEL 1280 TOTAL DOSE CKT

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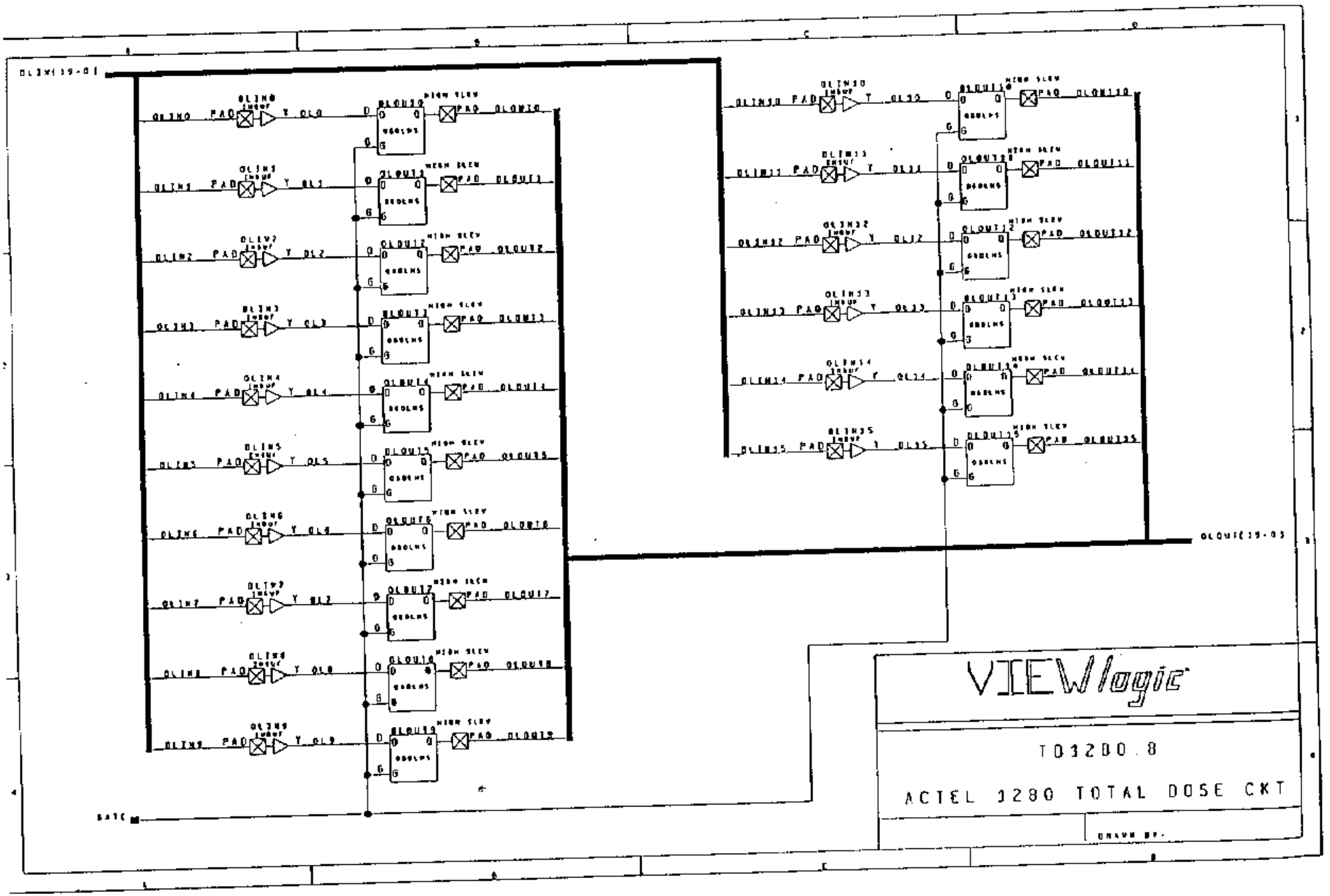
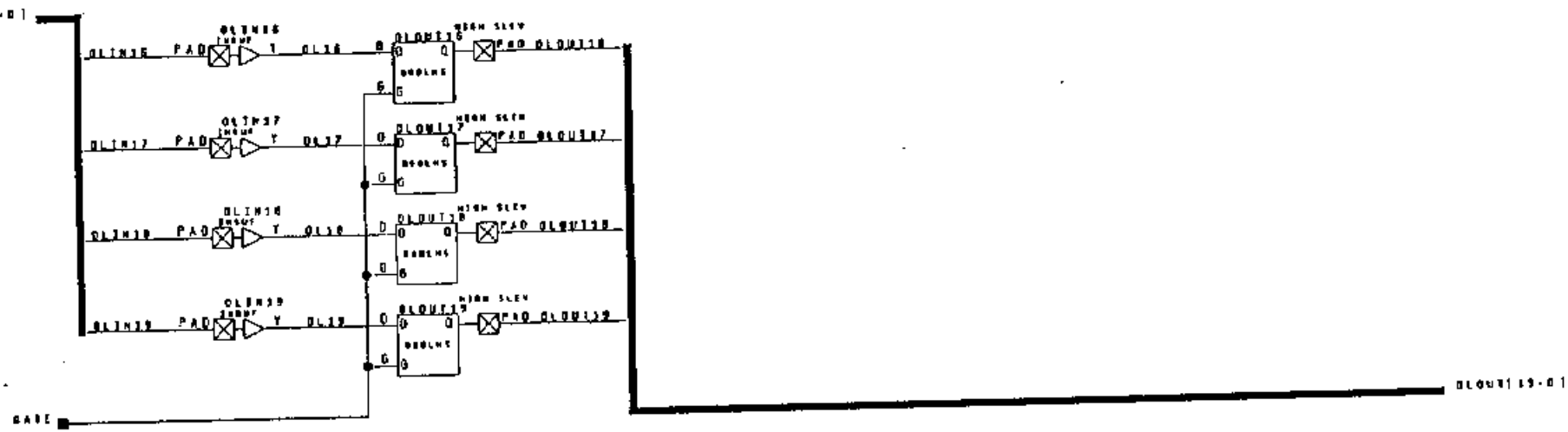

VIEWlogic
TD1280.8
ACTEL 1280 TOTAL DOSE CKT



VIEWlogic

T01280.9

ACTEL 1280 TOTAL DOSE CKT

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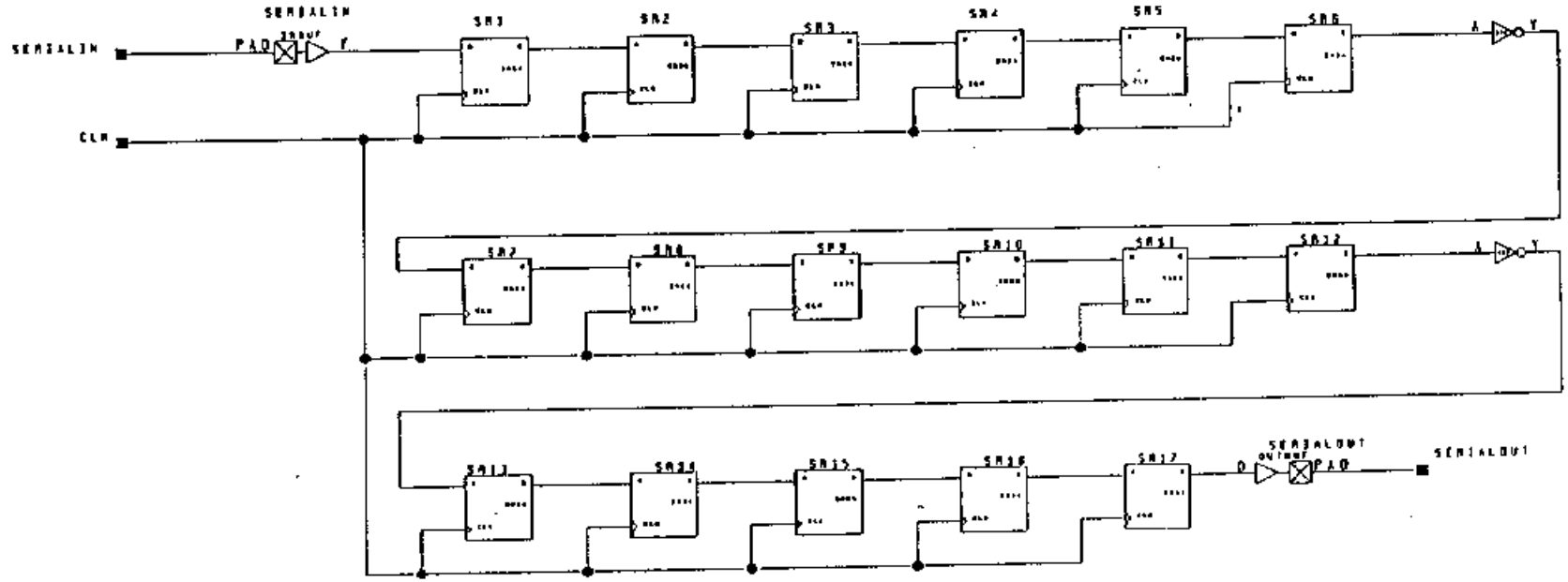
-A11-



VIEWlogic

T01200.10

ACTEL 1280 TOTAL DOSE CKT

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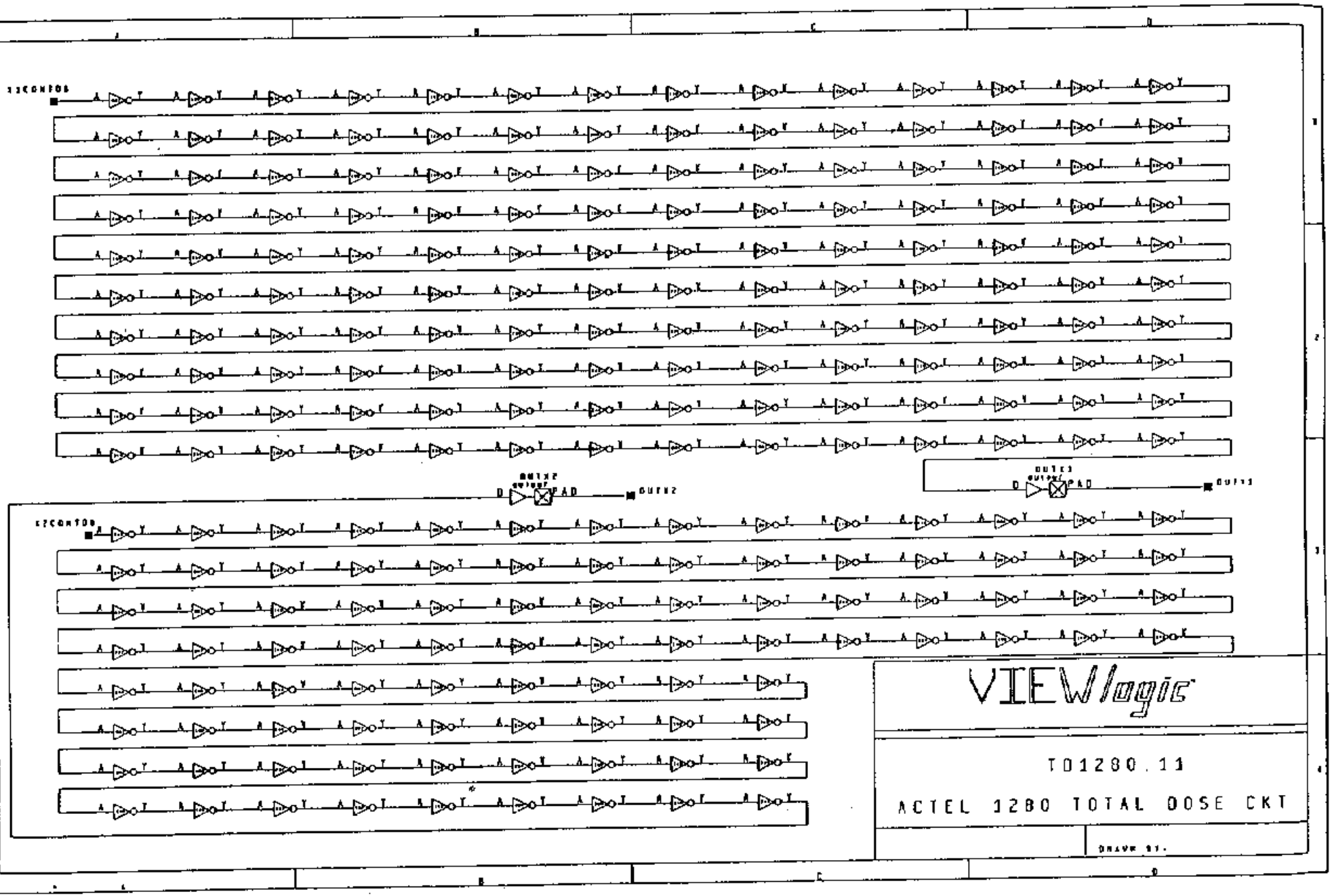
VIEWlogic
T01280.11
ACTEL 1280 TOTAL DOSE CKT