PPM-91-390

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UNISYS

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Interoffice Memorandum

PPM-91-390

To
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Department
Code 300.1
From
K. Sahu K-S
Department
7809
Subject
Radiation Report on ISTP
Non-Common Buy Part No. AD7224UQ/883B

Date
June 13, 1991
Location
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Telephone
731-8954
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A radiation evaluation was performed on AD7224UQ to determine the total dose tolerance of these parts. A brief summary of the test results is provided below. For detailed information, refer to Tables I through IV and Figure 1.

The total dose testing was performed using a cobalt-60 gamma ray source. During the radiation testing, eight parts were irradiated under bias (see Figure 1 for bias configuration), and two parts were used as control samples. The total dose radiation steps were 2.5, 5, 10, 15 and 20 krads. After 20 krads, parts were annealed at 25°C for 24 hours. The dose rate was between 125 - 250 rads/hour, depending on the total dose level (see Table II for radiation schedule). After each radiation exposure and annealing treatment, parts were electrically tested according to the test conditions and the specification limits listed in Table III. See Appendix I for a description of each test performed.

All (8) parts passed all tests up to 2.5 krads. After 5 krads exposure, one part (SN 259) failed Zero Code Error 1 (ZCE1) with a reading of 32.1mV against the upper specification limit of 30mV. After 10 krads irradiation, six parts failed ZCE1 with readings ranging from 27mV to 762mV. In addition, parts began failing Fullscale Error, DBx Error, SUM INL-, DBx Carry Error, and SUM DNL± and some of the Truth Table functional tests. After 15 krads, parts began failing ZCE2, and continued degradation in all of the above parameters was observed. Parts continued to deteriorate after 20 krads and no significant recovery was observed after annealing the parts for 24 hours. In contrast to the above tests, all parts passed all input leakage current tests up to 20 krads. Table IV provides the mean and standard deviation values for each parameter after different radiation exposures and annealing treatments. It also provides a summary of functional test results after each radiation/annealing step.

Any further details about this evaluation can be obtained upon request. If you have any questions, please call me at 301-731-8954.

TABLE I. Part Information

Generic Part Number:	AD7224UQ
ISTP Non-Common Buy Part Number:	AD7224UQ/883B
ISTP Non-Common Buy Control Number:	1992
Charge No. :	C03875
Manufacturer:	Analog Devices
Quantity Procured:	38
Lot Date Code:	8919
Quantity Tested:	10
Serial Numbers of Radiation Samples:	252, 253, 254, 255, 256, 257, 258, 259
Serial Numbers of Control Samples:	250, 251
Part Function:	8 Bit D/A Converter
Part Technology:	CMOS
Package Style:	18 Pin DIP

TABLE II. Radiation Schedule

EVENTS	DATE
1) Initial Electrical Measurements	04/01/91
2) 2.5 krads irradiation @ 125 rads/hr	04/01/91
Post 2.5 krads Electrical Measurements	04/02/91
3) 5 krads irradiation @ 125 rads/hr	04/02/91
Post 5 krads Electrical Measurements	04/03/91
4) 10 krads irradiation @ 250 rads/hr	04/03/91
Post 10 krads Electrical Measurements	04/04/91
5) 15 krads irradiation @ 250 rads/hr	04/04/91
Post 15 krads Electrical Measurements	04/05/91
6) 20 krads irradiation @ 250 rads/hr	04/08/91*
Post 20 krads Electrical Measurements	04/09/91
7) 24 hrs annealing	04/09/91
Post 24 hr Electrical Measurements	04/10/91

* The cumulative radiation step of 20 krads was scheduled to begin on 04/05/91; however, the radiation facility was not available until 04/08/91. The parts were kept under bias from 04/05/91 to 04/08/91.

Notes:

- All parts were radiated under bias at the cobalt-60 gamma ray facility at GSFC.
- All electrical measurements were performed off-site at 25°C.
- Annealing performed at 25°C under bias.

Table III. Electrical Characteristics of AD7224UQ

TEST#	DESCRIPTION	MIN	MAX
1	IDD @ 16.5V	0.4ma	4ma
2	ISS @ -5.5V	-3ma	-0.3ma
3.X	Zero Code Error	-30mv	30mv
4	Fullscale Error (Dual)	-1.5LSB	1.5LSB
5	Total Unadjusted Error (Dual)	-2LSB	2LSB
6	Differential Nonlinearity (Dual)	-1LSB	1LSB
7	Input Leakage @ 0V	-1ua	1ua
8	Input Leakage @ 11.4V	-1ua	1ua
9	Total Unadjusted Error (Single)	-2LSB	2LSB
10	Differential Nonlinearity (Single)	-1LSB	1LSB
11	Input Leakage @ 0V	-1ua	1ua
12	Input Leakage @ 14.25V	-1ua	1ua
13	IDD @ 15.75V	0.6ma	6ma
14	Truth Table Functional	---	----

Table IV. Summary of Electrical Measurements
after Total Dose Exposures and Annealing for AD7224UQ/883 1/, 2/, 3/, 4/

Parameters	Spec. Limits min	Spec. Limits max	Initials mean	Initials sd	Total Dose Exposure (krads) 2.5 mean	2.5 sd	5 mean	5 sd	10 mean	10 sd	15 mean	15 sd	20 mean	20 sd	Annealing 24 hrs. mean	Annealing 24 hrs. sd
IDD @15.5V mA	0.4	4.0	2.3	0.1	2.3	0.1	2.3	0.1	2.4	0.1	3.1	0.1	3.2	0	3.1	0
ISS @-5.5V mA	-3.0	-0.3	-1.7	0.1	-1.6	0.1	-1.6	0.1	-1.5	0.1	-1.5	0.1	-1.5	0.1	-1.5	0.1
ZCE1 mV	-30	30	-3.3	4.0	2.0	3.0	20.0	4.0	150	200	400	100	765	5	765	5
ZCE2 mV	-30	30	-1.0	3.0	0.5	2.0	1.5	2.0	9.0	2.0	220	80	375	120	378	122
FS Error LSB	-1.5	1.5	1.30	.07	1.43	.01	0.9	0.4	1.73	0.4	2.9	0.4	4.8	0.6	4.2	0.7
DB1 bitE LSB	-2	2	0.1	0.1	0.1	0.1	-0.1	0.1	-4.0	4.0	-7.7	3.0	-15.5	0.1	-14.0	5.0
Sum INL+ LSB	-2	2	1.8	0.7	1.0	1.0	0.6	0.2	0.2	0.1	0.2	0.1	0	0	0	0
Sum INL- LSB	-2	2	0	0	-0.1	0.1	-0.6	1.0	-13.0	30.0	-80	25	-113	1	-100	20
DB0 carryE LSB	-1	1	0.2	0.1	0.3	0.1	0.3	0.1	2.3	4.0	6.5	3.0	16.0	0.1	14.0	2.0
Sum DNL+ LSB	-1	1	0.6	0.1	0.78	.05	0.57	0.10	8.0	15.0	40	13	66	4	58	9
Sum DNL- LSB	-1	1	-0.1	0	-0.1	0	-0.1	0	-0.4	0.5	-2.0	0.8	-3.8	0.5	-3.8	0.5
DB0 IIL uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/Reset IIL uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/LDAC IIL uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/WR IIL uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/CS IIL uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

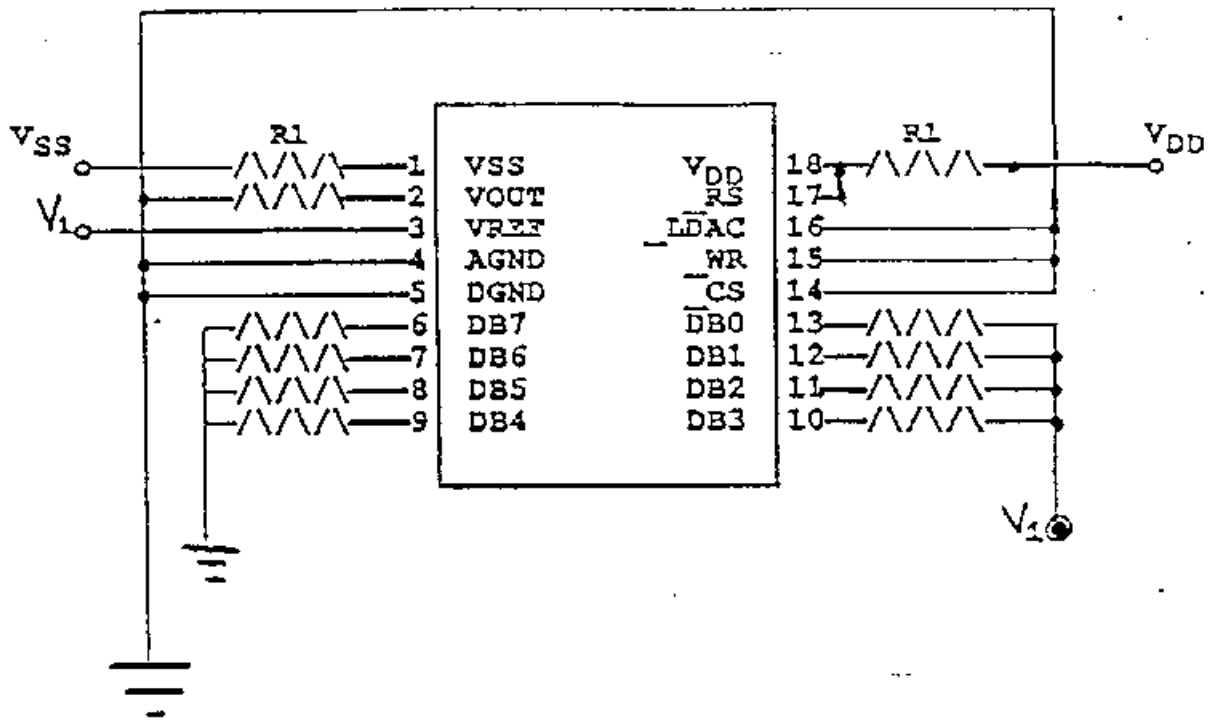
(Table IV continued on next page)

Table IV. (continued)

Parameters	Spec. Limits min	Spec. Limits max	Initials mean	Initials sd	Total Dose Exposure (krads) 2.5 mean	2.5 sd	5 mean	5 sd	10 mean	10 sd	15 mean	15 sd	20 mean	20 sd	Annealing 24 hrs. mean	Annealing 24 hrs. sd
DB0 IIH uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/Reset IIH uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/LDAC IIH uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/WR IIH uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
/CS IIH uA	-1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Truth #1	9.9	10.1	Pass		Pass		Pass		Pass		7P/1F		4P/4F		3P/5F	
Truth #2	9.9	10.1	Pass		Pass		Pass		Pass		7P/1F		4P/4F		4P/4F	
Truth #3	9.9	10.1	Pass		Pass		Pass		Pass		7P/1F		3P/5F		3P/5F	
Truth #4	9.9	10.1	Pass		Pass		Pass		Pass		7P/1F		3P/5F		3P/5F	
Truth #5	9.9	10.1	Pass		Pass		Pass		Pass		7P/1F		4P/4F		3P/5F	
Truth #6	6.9	7.1	Pass		Pass		Pass		7P/1F		4P/4F		Fail		Fail	
Truth #7	6.9	7.1	Pass		Pass		Pass		7P/1F		4P/4F		Fail		Fail	
Truth #8	-0.1	0.1	Pass		Pass		Pass		6P/2F		1P/7F		Fail		Fail	
Truth #9	-0.1	0.1	Pass		Pass		Pass		6P/2F		1P/7F		Fail		Fail	
Truth #10	0.9	1.1	Pass		Pass		Pass		6P/2F		4P/4F		Fail		Fail	

Notes:
1/ The mean and standard deviation values were calculated over the eight parts irradiated in this testing. The control samples remained constant throughout the testing and are not included in this table.
2/ The tests listed in Table IV were performed with VSS = -5V (Dual Supply). Single supply (VSS = 0V) tests were also performed and these tests showed similar degradation in the same parameters as above. This data is available and can be obtained upon request.
3/ Table IV lists the number of parts which passed or failed each of the Truth Table tests. A part was considered to have failed such a test if its reading was outside that of the passing range (ie. 9.89V is a failing reading for Truth Table test#1.
4/ Some of the parameters tested are not included in Table IV; however, the parametric data included in Table IV is representative of all the test data. For example, test data on IDD @15.75V was similar to that of IDD @16.5V, and test data on Data Bit Error 2 through 8 was similar to that of DB1 Error.

Figure 1. Radiation Bias Circuit for AD7224UQ



NOTE: V_{DD} is turned on first, then V_{SS} followed by V_{REF}

2. V_{DD} = 15.0 ± 0.5 Volts

3. V_{SS} = -5.0 ± 0.25 Volts

4. VI = +5.0 ± 0.25 Volts

5. R1 = 100 Ohms, 5%, 1/4 watts
   All other resitors are 2k Ohms, 5%, 1/4 watts

Appendix I

Test# 1 IDD @ 16.5V 4ma Max

VDD is set to 16.5 volts,VSS is set to -5.5V and Vref is set to 12.5 volts. All input bits are turned on to provide the maximum current draw. The current of VDD is measured.

Test# 2 ISS @ -5.5V -3ma Max

VDD is set to 16.5 volts,VSS is set to -5.5V and Vref is set to 12.5 volts. All input bits are turned on to provide the maximum current draw. The current of VSS is measured.

Test# 3.X Zero Code Error (Dual) 30mv Max

VDD is set to 16.5 volts, Vref is set to 12.5 volts and VSS is set to -5 volts. The DAC output is measured with all bits off. The output voltage is measured. Test#3.2 has VDD changed to 11.4V and Vref to 7.4V. Output is then measured. Test#3.3 has VDD changed to 14V and Vref to 10V. The output is then measured.

Test# 4 Fullscale Error (Dual) 1.5LSB Max

VDD is set to 14 volts. The DAC output is measured with all inputs bits on. The theoretical value is subtracted from the measured value. The difference is scaled in terms of LSB.

Test# 5 Total Unadjusted Error (Dual) 2LSB Max

Input code is set to 1 and the voltage out is measured. The theoretical value is subtracted from the measured value and the result is expressed in LSB. DB1 is turned off and DB2 is turned on and the output measured. This is done for all 8 bits. The positive and negative sums are calculated.

Test# 6 Differential Linearity 1 LSB Max

Differential Linearity compares the change in the output, due to one code increment at the input, with the theoretical step size. The DAC outputs for all Major Carry Pairs are measured. Their differences are compared to an LSB based on the DAC's fullscale value. The error is scaled in terms of LSB's. The positive and negative sums are calculated.

Test# 7 Digital Input Leakage @ 0V 1ua Max

VDD is set to 11.4V, VSS to -5V. All input bits are set to 11.4V except the pin under test. The pin under test is set to 0 volts. The current out is measured using the current sense resistors. All input bits are tested this way.

Test# 8 Digital Input Leakage @ 11.4V 1ua Max

VDD is set to 11.4V, VSS to -5V. All input bits are set to 0V except the pin under test. The pin under test is set to 11.4 volts. The current out is measured using the current sense resistors. All input bits are tested this way.

Test# 9 Total Unadjusted Error (Single) 2LSB Max

VDD is set to 14V, VSS set to 0v and VREF to 10V. Input code is set to 1 and the voltage out is measured. The theoretical value is subtracted from the measured value and the result is expressed in LSB. DB1 is turned off and DB2 is turned on and the output measured. This is done for all 8 bits. The positive and negative sums are calculated.

Test# 10 Differential Linearity (Single) 1 LSB Max

Differential Linearity compares the change in the output, due to one code increment at the input, with the theoretical step size. The DAC outputs for all Major Carry Pairs are measured. Their differences are compared to an LSB based on the DAC's fullscale value. The error is scaled in terms of LSB's. The positive and negative sums are calculated.

Test# 11 Digital Input Leakage @ 0V 1ua Max

VDD is set to 14.25V, VSS to 0V. All input bits are set to 14.25V except the pin under test. The pin under test is set to 0 volts. The current out is measured using the current sense resistors. All input bits are tested this way.

Test# 12 Digital Input Leakage @ 14.25V 1ua Max

VDD is set to 14.25V, VSS to 0V. All input bits are set to 0V except the pin under test. The pin under test is set to 14.25 volts. The current out is measured using the current sense resistors. All input bits are tested this way.

Test# 13 IDD @ 15.75V 6ma Max

VDD is set to 15.75 volts,VSS is set to 0V and Vref is set to 10 volts. All input bits are turned on to provide the maximum current draw. The current of VDD is measured.

Test# 14 Truth Table Functional

The truth table on page 6 of the spec is tested.

T#14.01 has the input code set to have 10V out and the register logic set for transparent mode. The output should be 10V.

T#14.02 has the register logic set for latched mode 1 and input code set to have 9V out. The output should stay 10V.

T#14.03 has the register logic set for latched mode 2 and input code set to have 8V out. The output should stay 10V.

T#14.04 has the register logic set for input register transparent mode and input code set to have 7V out. The output should stay 10V. Input register now has 7V code in it.

T#14.05 has the register logic set for input register latched mode and input code set to have 6V out. The output should stay 10V. Input register now has 7V code latched in it.

T#14.06 has the register logic set for DAC register transparent mode and input code set to have 5V out. The output should go to 7V.

T#14.07 has the register logic set for DAC register latched mode and input code set to have 4V out. The output should stay 7V.

T#14.08 has the register logic set for both registers loaded with zero's and input code set to have 3V out. The output should go to 0V.

T#14.09 has the register logic set for both registers latched with zero's and input code set to have 2V out. The output should stay at 0V.

T#14.10 has the register logic set for both registers transparent and input code set to have 1V out. The output should go to 1V.