Proton Tolerance of Multiple-Threshold Voltage and Multiple-Breakdown Voltage CMOS Device Design Points in a 0.18 µm System-on-a-Chip CMOS Technology

Ying Li[1], John D. Cressler[2], Yuan Lu[2], Jun Pan[1], Guofu Niu[1], Robert A. Reed[3], Paul W. Marshall[4], Christopher Polar[5], Michael J. Palmer[1] and Alvin J. Joseph[6]

[1]Alabama Microelectronics Science and Technology Center, Electrical and Computer Engineering Department, 200 Broun Hall, Auburn University, Auburn, AL 36849, USA.
[2]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA.
[3]NASA-GSFC, Code 562, Greenbelt , MD 20771, USA.
[4]Consultant to NASA-GSFC, Code 562, Greenbelt, MD 20771, USA.
[5]Jackson and Tull Chartered Engineers, Washington, DC 20018, USA.
[6]IBM Microelectronics, Essex Junction, VT 05401 USA.

35-Word Abstract

The paper presents the first investigation of the proton radiation response of the *dc* and *RF* performance of the multiple CMOS device design points in a 0.18 µm system-of-a-chip CMOS technology.

Author Contact Information:

Ying Li
200 Broun Hall, Electrical and Computer Engineering Department, Auburn University, Auburn, AL, 36849, USA
Tel: (334) 844-1865 / Fax: (334) 844-1888 / E-mail: yingli@eng.auburn.edu.

Submitted to:

Radiation Effect Data Workshop

Student Paper

Proton Tolerance of Multiple-Threshold Voltage and Multiple-Breakdown Voltage CMOS Device Design Points in a 0.18μm System-on-a-Chip CMOS Technology

Ying Li, John D. Cressler, Yuan Lu, Jun Pan, Guofu Niu, Robert A. Reed, Paul W. Marshall, Christopher Polar, Michael J. Palmer and Alvin J. Joseph

Abstract— **The paper presents the first investigation of the proton tolerance of the multiple-threshold voltage and multiple-breakdown voltage device design points contained in a 0.18μm system-of-a-chip CMOS technology. The radiation response of the CMOS devices having three different device design configurations are characterized and compared for equivalent gamma doses up to 300 krad(Si), using the threshold voltage, off-state leakage, and effective mobility to assess *dc* performance. All three CMOS device configurations show a very slight degradation of threshold voltage and effective mobility with increasing dose. We also present for the first time the frequency response and S-parameters of these RF CMOS devices under proton radiation. The S-parameters and cut-off frequency show little degradation up to 300 krad(Si) total dose. These results suggest that the CMOS devices in this 0.18μm SoC CMOS technology are well-suited for RF circuit applications in a radiation environment without intentional total-dose hardening.**

I. Introduction

It is well known that CMOS scaling improves the transistor frequency response, and scaled CMOS technologies are being increasingly used to address low-end (1-2 GHz) RF transceiver IC applications for low-cost wireless systems. Clearly, however, RFIC design places much more stringent demands on device performance and hence traditional core CMOS technologies used in digital logic are not well-suited to RF CMOS implementations. Because of this, so-called "system-on-a-chip" (SoC) CMOS technologies [1] have recently emerged, and contain multiple CMOS device design points in order to address multiple application arenas, and include, for instance, RF CMOS (thick oxide, high V_{DD}), high-speed digital logic (thin oxide, nominal V_{th}), and low-power digital logic (thin oxide, high V_{th}), all in the same technology core. This emerging SoC CMOS trend is clearly of importance to the space community, since high levels of integration and low cost are of increasing importance for space missions. For such an SoC CMOS technology to present a viable option for space, however, its radiation tolerance obviously must be carefully scrutinized. In this paper, we investigate for the first time the proton radiation response of the *dc* and *RF* performance of the multiple CMOS device design points in a 0.18μm SoC CMOS technology.

This work was supported DTRA under the Radiation Tolerant Microelectronics Program, NASA-GSFC under the Electronics Radiation Characterization Program, and NASA Jet Propulsion Laboratory under the CISM program.

Y. Li, J. Pan, G. Niu, M.J. Palmer are with the Alabama Microelectronics Science and Technology Center, Electrical and Computer Engineering Department, 200 Broun Hall, Auburn University, Auburn, AL 36849, USA. Tel: (334) 844-1865 / Fax: (334) 844-1888 / E-mail: yingli@eng.auburn.edu.

J. D. Cressler and Y. Lu is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA.

R. A. Reed is with NASA-GSFC, Code 562, Greenbelt , MD 20771, USA.

P. W. Marshall is a consultant to NASA-GSFC, Code 562, Greenbelt, MD 20771, USA.

C. Polar is with Jackson and Tull Chartered Engineers, Washington, DC 20018, USA.

A. Joseph is with IBM Microelectronics, Essex Junction, VT 05401 USA.

II. Experiment

The CMOS devices under investigation are contained in a commercially-available 0.18μm CMOS technology. The basic CMOS fabrication process in this is as follows: after subcollector and epilayer formation, the deep- and shallow-trench isolation are completed. CMOS wells are then implanted, followed by gate oxidation, poly gate and spacer formation, and LDD implants [2]. This CMOS technology was not radiation-hardened in any way. Table. I shows the parameters of test devices in three different configurations (design points): 0.18 μm 1.8 V nominal V_{th} (for high speed digital logic), 0.18 μm 1.8 V high V_{th} (for low power digital logic), and a thick oxide, 0.30 μm 3.3 V RF CMOS. The gate oxide is 3.5 nm for the 1.8 V nominal/high V_{th} configurations, while for the 3.3 V RF CMOS, the device has 6.8 nm gate oxide thickness. For each device design point, three different sizes of devices were investigated: 1) 10/0.18 (W/L=10μm/0.18μm), 10/0.24, and 10/10 nFETs for 1.8 V nominal/high V_{th}; 10/0.30, 10/0.40 and 10/10 nFETs for the 3.3 V RF CMOS configuration. The pFETs were radiation hard and for brevity are not discussed here.

TABLE I
Parameters of Test Devices

Device Design Point	t_{ox} (nm)	V_{DD} (V)	V_{th} (V) (L)
1.8 V nominal V_{th}	3.5	1.8	0.50 (0.18μm)
1.8 V high V_{th}	3.5	1.8	0.65 (0.18μm)
3.3 V configuration	6.8	3.3	0.69 (0.30μm)

Samples for *dc* measurements were mounted in 24 pin DIP packages, wire-bonded, and then exposed to 62.5MeV protons up to 300 krad(Si) equivalent gamma dose at the Crocker Nuclear Laboratory Cyclotron located at the University of California at Davis. During irradiation, the devices were biased in the "ON-gate" configuration (V_{GS}=V_{DD}, V_D=V_S=V_{sub}=0) to realize worst-case conditions. The *dc* characteristics of the test devices were measured pre-radiation and immediately after each radiation dose using an Agilent 4155 Semiconductor Parameter Analyzer. The samples for the *ac* measurements were mounted on ceramic holders and exposed to proton radiation up to 300 krad(Si) equivalent gamma dose with terminal floating (the only possibility to facilitate post-radiation broadband measurements). An HP8510C Vector Network Analyzer was used for scattering parameter (S-parameter) measurements before and after irradiation.

III. Results and Discussion

A. dc performance

Fig. 1 shows the pre- and post-radiation drain current (I_D) versus gate voltage (V_{GS}) characteristics for a 10/0.18 nFET in 1.8 V nominal V_{th} configuration. The same I_D is plotted on a logarithmic scale on the left y-axis, and on a linear scale on the right y-axis. It is clearly shown that the off-state leakage increases from $10pA$ before radiation to about $90nA$ after 300 krad. This off-state leakage is attributed to the device region where the gate overlaps the shallow trench isolation, where a parasitic inversion channel is produced at sufficiently high damage, resistively shunting the source to the drain. Clearly, however, this device technology is robust to total-dose exposure up to at least 150 krad. Observe that here is almost no degradation in the linear $I_D - V_{GS}$ characteristics in this 10/0.18 nFET. Fig. 1 shows that the radiation-induced threshold voltage and transconductance degradation is negligible, as expected, since this device has very thin, high-quality gate oxide (3.5 nm in this case). Similar results can also be seen for the 10/0.18 nFET in 1.8 V high V_{th} configuration with the same gate oxide thickness but the higher pre-radiation threshold voltage.

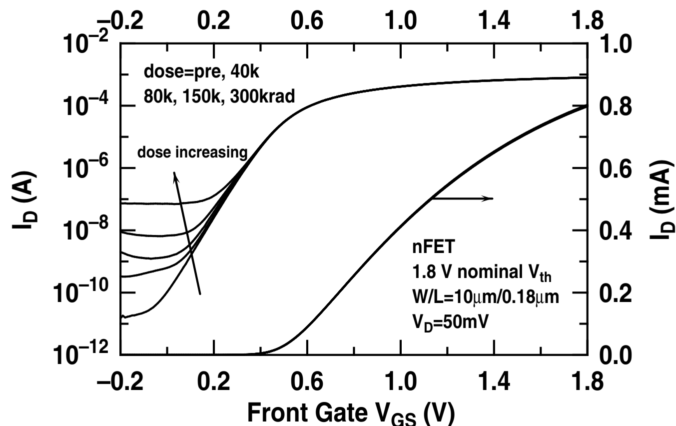

Fig. 1. Front-gate subthreshold characteristics of a 10/0.18 nFET in 1.8 V nominal V_{th} configuration before and after radiation.

To more closely examine the radiation-induced off-state leakage of the nFETs in the three different device configurations, we chose devices with identical geometry (10/10) for ease of comparison. As shown in Fig.2, the normalized off-state leakage of the 10/10 nFET in the 3.3 V RF CMOS configuration increases much more quickly than in both the 1.8 V nominal V_{th} and the 1.8 V high V_{th} configurations, which is attributed to the reduced gate control on the shallow trench isolation edge in the 3.3 V RF CMOS configuration, due to its thicker gate oxide [3]. That is, for the same amount of STI damage, the gate cannot as effectively deplete that parasitic leakage channel if the gate oxide thickness is increased.

Fig. 3 compares the radiation-induced threshold voltage shift (ΔV_{th}=$V_{th,post}$-$V_{th,pre}$) for the same 10/10 nFETs shown in Fig. 2 for the three different device configurations. Although ΔV_{th} is small for all three devices, we can still see that the 10/10 nFET in the 3.3 V RF CMOS configuration has a larger threshold voltage shift (30mV at 300 Krad) than the other two configurations

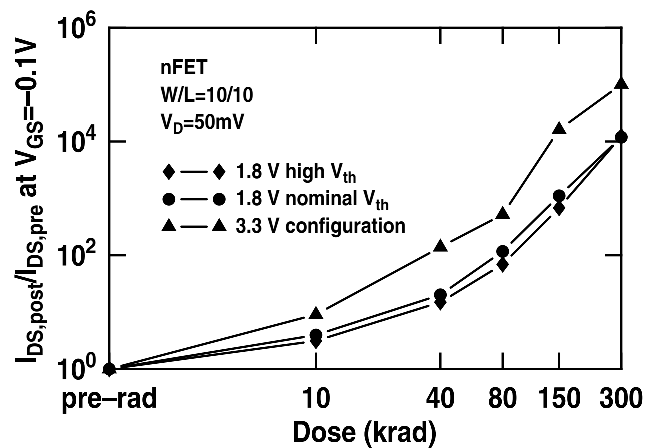

Fig. 2. Normalized off-state leakage for the 10/10 nFETs in the three device configurations as a function of equivalent total dose.

(around 11mV at 300 Krad), because the radiation damage on the thicker gate oxide (6.8nm) of 3.3 V RF CMOS configuration is much stronger than the thin gate oxide (3.5nm) found in the two 1.8 V configurations. The ΔV_{th} of 1.8 V nominal V_{th} device is comparable with that of 1.8 V high V_{th} device, although a slightly higher due to the lower pre-radiation value of V_{th}.

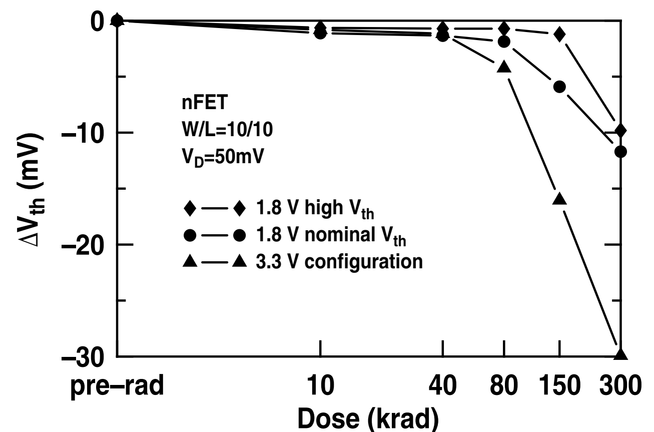

Fig. 3. The threshold voltage shift for the 10/10 nFETs in the three configurations as a function of equivalent total dose.

The effective channel mobilities (μ_{eff}) for these three device configurations were extracted as a function of gate overdrive using a recently proposed technique which is capable of taking into account the bias dependence of R_{SD} in LDD CMOS technologies [4]. The results are shown in Fig. 4 for both pre-radiation and after 300 krad total dose. The change of μ_{eff} after irradiation is negligible for all three configurations. With increasing $V_{GS} - V_{th}$ (i.e. vertical field), μ_{eff} decreases rapidly, as expected. At the $V_{GS} - V_{th}$=0.6V, μ_{eff} is 275, 305 and 330 $cm^2/(Vs)$ for 1.8 V high V_{th}, 1.8 V nominal V_{th} and 3.3 V RF CMOS configurations, respectively. The 1.8 V high V_{th} device has the smallest effective mobility due to the heavier doping in the channel required to reach the higher V_{th} value compared with the 1.8 V nominal V_{th}, while the 3.3 V RF CMOS configuration has the largest effective mobility due to the thicker gate oxide.

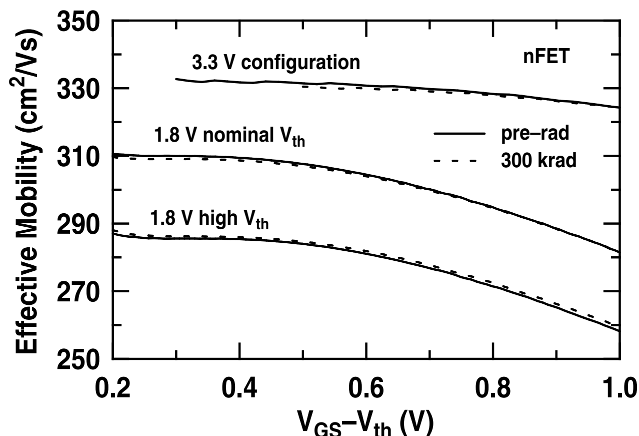

Fig. 4. Effective channel mobility versus gate overdrive for the three configurations at pre-radiation and after 300 krad.

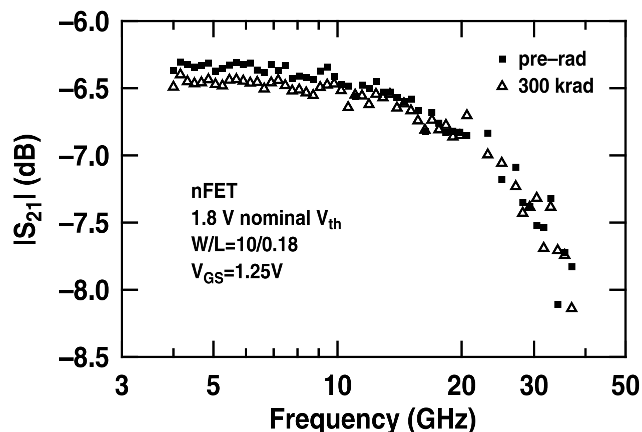

Fig. 6. S_{21} magnitude versus frequency at V_{GS}=1.25V for the 10/0.18 nFET at pre-radiation and after 300 krad.

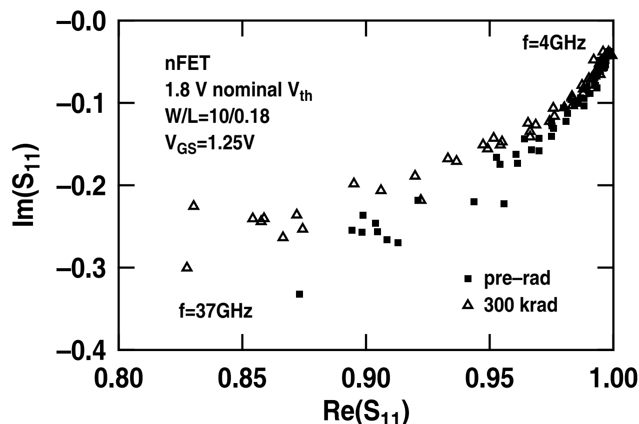

Fig. 5. Comparison of Re(S_{11}) and Im(S_{11}) at pre-irradiation and after 300 krad exposure.

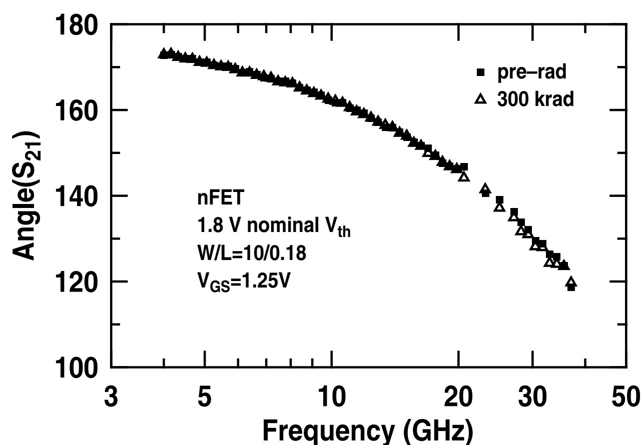

Fig. 7. Angle(S_{21}) versus frequency at V_{GS}=1.25V for the 10/0.18 nFET at pre-radiation and after 300 krad.

B. RF performance

S-parameters are most commonly used to characterize the electrical response of high frequency transistors. The RF figures-of-merit of the transistors can be extracted from the measured S-parameters of the transistor, after appropriate parasitic deembedding. The typical radiation response of the four S-parameters up to 300 krad in a 10/0.18 nFET of 1.8 V nominal V_{th} configuration is shown in Fig. 5 through Fig. 10. The other device configurations show a similar response. Fig. 5 shows the comparison of Re(S_{11}) and Im(S_{11}) before radiation and after 300 krad. We see that the S_{11} for the nFET always moves clockwise as frequency increases from 4GHz to 37GHz because the S_{11} is the reflection coefficient corresponding to the input impedance when the output is terminated with the characteristic impedance Z_0. After 300 krad radiation, there is only a slight increase of the S_{11}, which can be considered negligible.

Fig. 6 and Fig. 7 show the magnitude of S_{21} and the angle of S_{21} as a function of frequency at pre-irradiation and after 300 krad, respectively. The S_{21} magnitude decreases with increasing frequency, as expected, because of decreasing forward transducer gain. A small decrease of the S_{21} magnitude can be observed in Fig. 6 after 300 krad radiation, however there are no changes in the angle of S_{21} after radiation (Fig. 7).

S_{12}, the reverse gain, increases with increasing frequency, as shown in Fig. 8, which shows its magnitude versus frequency. No radiation-induced degradation can be observed for both the S_{11} magnitude in Fig. 8 and the angle of S_{11} in Fig. 9.

S_{22} is essentially the output reflection coefficient looking back into the output port for a Z_0 source termination. The radiation response of S_{22} can be seen in Fig. 10. Both ReS_{22} and ImS_{22} decrease after radiation, though only slightly.

From an RF CMOS perspective, all of the S-parameters experience negligible degradation after 300 krad total dose exposure, suggesting that this RF CMOS technology is radiation hard for the applications in the proton environment. The cut-off frequency f_T can be extracted from the measured S-parameters. For this 10/0.18 nFET presented above, the peak f_T is 55 GHz at pre-radiation and 53 GHz after 300 krad, yielding a negligible change in overall frequency response, as expected. The cut-off frequency f_T of a 10/0.40 nFET in 3.3 V configuration is shown in Fig. 11 before and after radiation. Only a slight decrease of f_T can be observed for this 3.3 V configuration device after radiation. The peak f_T is 23.5 GHz at pre-radiation and 23 GHz after 300 krad.

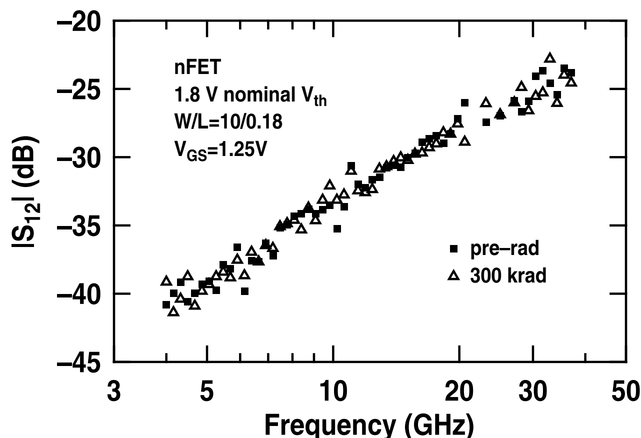

Fig. 8. S_{12} magnitude versus frequency at V_{GS}=1.25V for the 10/0.18 nFET at pre-radiation and post-radiation.

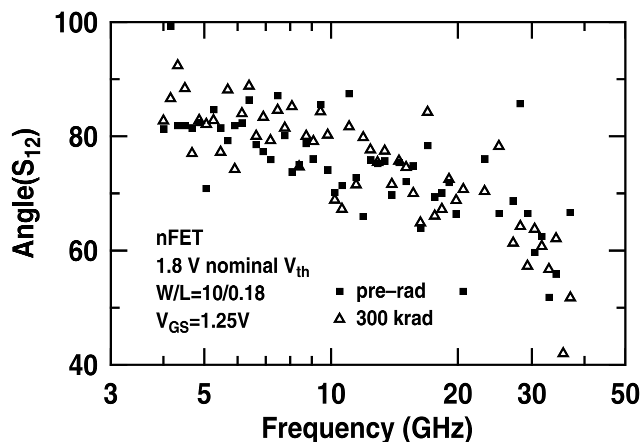

Fig. 9. Angle(S_{12}) versus frequency at V_{GS}=1.25V for the 10/0.18 nFET at pre-radiation and post-radiation.

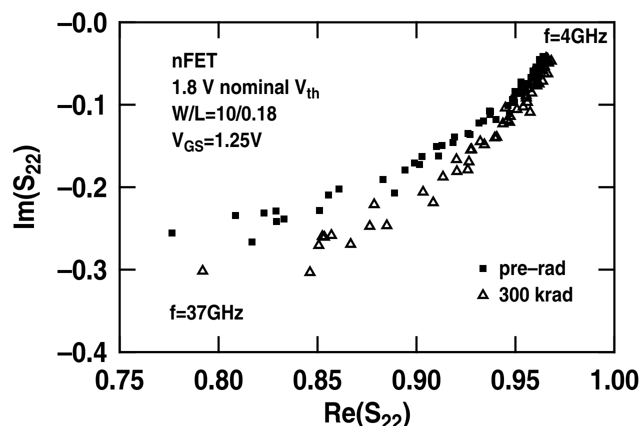

Fig. 10. Comparison of Re(S_{22}) and Im(S_{22}) at pre-radiation and after 300 krad.

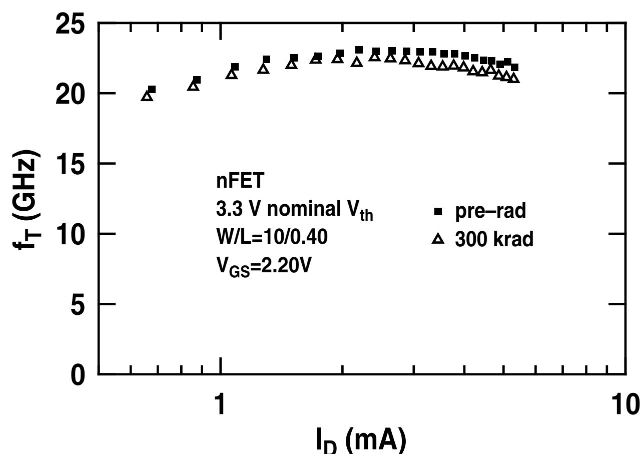

Fig. 11. The cut-off frequency as a function of drain current at pre-radiation and after 300 krad.

IV. Summary

The proton tolerance of the multiple-threshold voltage and multiple-breakdown voltage system-of-a-chip CMOS devices contained in a 0.18μm SoC CMOS technology are presented for the first time. The radiation response of the CMOS devices having three different device design configurations were characterized and compared for equivalent gamma doses up to 300 krad(Si), using the threshold voltage, off-state leakage, and effective mobility to assess *dc* performance. All three CMOS device configurations show a very slight degradation of threshold voltage and effective mobility with increasing dose. The transistor frequency response and S-parameters of these RF CMOS devices show little degradation up to 300 krad(Si) total dose. These results suggest that the CMOS devices in this 0.18μm SoC CMOS technology are well-suited for RF circuit applications in a radiation environment without intentional total-dose hardening.

Acknowledgment

The devices were fabricated at IBM Microelectronics. The authors would like to thank L. Cohn, K. LaBel, and H. Brandhorst for their support of this work.

References

[1] P.H. Woerlee, M.J. Knitel, R. Langevelde, D.B.M. Klaassen, L.F. Tiemeijer, A.J. Scholten, and A. Duijnhoven, "RF-CMOS Performance Trends," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1776-1782, Aug. 2001.

[2] A. Joseph, D. Coolbaugh, M. Zierak, R. Wuthrich, R. Geiss, Z. He, X. Liu, B. Orner, J. Johnson, G. Freeman, D. Ahlgren, B. Jagannathan, L. Lanzerotti, V. Ramachandran, J. Malinowski, H. Chen, J. Chu, P. Gray, R. Johnson, J. Dunn, S. Subbanna, K. Schonenberg, D. Harame, R. Groves, K. Watson, D. Jadus, M. Megheli, and A. Rylyakov, "A 0.18μm BiCMOS technology featuring 120/100 GHz (f_T/f_{max}) HBT ans ASIC-compatible CMOS using copper Interconnect," *Proceedigns of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 143-146, 2001.

[3] J.D. Cressler, R. Krithivasan, G. Zhang, G. Niu, P. W. Marshall, H.S. Kim, R.A. Reed, M.J. Palmer, and A.J. Joseph, "An investigation of the origins of the variable proton tolerance in multiple SiGe HBT BiCMOS technology generations," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 3203-3207, Dec. 2002.

[4] G. Niu, J.D. Cressler, S.J. Mathew, and S. Subbanna, "Total Resistance Slope-based Effective Channel Mobility Extraction Method for Deep Submicrometer CMOS Technology," *IEEE Transactions on Electron Devices*, vol. 46, no. 9, pp. 1912-1914, Sept, 1999.