Current Single Event Effect Test Results for Candidate Spacecraft Electronics

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Abstract

We present both proton and heavy ion single event effect (SEE) ground test results for candidate spacecraft electronics. A variety of digital and analog devices were tested, including EEPROMs, DRAMs, and DC-DC Converters.

I. Introduction

As spacecraft and spacecraft designers increasingly utilize increasing number of commercial technology devices versus the more traditional radiation hardened (RH) components in order to meet stringent spacecraft requirements in such areas as volume, weight, power, cost and schedule, SEE ground testing has become a key in many spaceflight programs.

The objective of this study was to determine the Linear Energy Transfer (LET) threshold (the minimum LET value to cause an effect at a fluence of 1E7 particles/cm^2) and saturation cross section of candidate spacecraft electronics for Single Event Upset (SEU) and latchup (SEL) due to protons and heavy ions.

II. Test Techniques and Setup

A. Test Facilities

Heavy Ion experiments were performed at the Brookhaven National Laboratories (BNL) Single Event Upset Test Facility (SEUTF). The SEUTF utilizes a tandem Tandem Van De Graaf accelerator suitable for providing various ions and energies. Testboards containing the device under test (DUT) are mounted inside a vacuum chamber. Testing was performed with LET values ranging from 1.1-120 MeV*cm^2/mg, fluences from 1E6- 1E7 particles/cm*2*, and fluxes from 1E2 -1E5 particles/cm*2*/sec, all depending on device sensitivity. Ions used are listed in Table 1. Intermediate LETs were obtained by changing the angle of incidence of the DUT to the ion beam, thus changing the path length of the ion through the DUT. Energies and LETs varied slightly from multiple test dates over the calendar year.

Table 1 *Test Ions*

Ion	Energy, MeV	LET, MeV*cm^2/mg
C-12	98	1.45
F-19	140	3.45
Si-28	186	7.88
Cl-35	210	11.4
Ni-58	278	26.2
Br-79	286	37.2
I-127	320	59.7
Au-197	350	82.3

Proton SEE testing was performed at both the University of California at Davis (UCD) and the University of Indiana at Bloomington (IUCF) cyclotron facilities. Test energies ranged from 26.6 to 63 MeV at UCD, and 54 to 197 MeV at IUCF. Typically, fluence was 1E10-1E11 particles/cm^2, and flux was 1E8 particles/cm^2/sec.

B. Test Method

Three modes of testing were used, depending on the DUT:

dynamic - actively exercise a DUT during beam exposure while counting errors, generally by comparing DUT output with a reference device or other expected output. Devices may have several dynamic test modes, such as *Read/Write* and *Read Only*, depending on their function.

static - load device prior to beam irradiation, then retrieve data post-run, counting errors

biased (SEL only) - DUT is biased and clocked while I_{cc} (power consumption) is monitored for SEL conditions.

Devices were monitored for both SEU (*transients*, *bit flips*,*control errors*, *etc.*, as defined on a device-by-device basis) and SEL (both *destructive* -- I_{cc} above specified maximum for the device -- and *microlatch* -- a self-limiting latchup localized to an area of the device; I_{cc} is above normal operating current, but below specified maximum for the device, requiring a power reset to clear).

All tests were performed at room temperature.

III. Test Results

Table 2 provides a list of the devices tested and summarizes the results: (H = Heavy Ion, P = Proton, SEU = SEU LET_{th}, SEL = SEL LET_{th}). All LETs are given in MeV*cm^2/mg in the table and in the discussion of test results which follows. This is only a summary of results; complete test reports are available online at http://flick.gsfc.nasa.gov/radhome.htm.

Table 2 *Devices Under Test and Results Summary*

DEVICE	FUNCTION	MANUF.	PROCESS	TEST RESULTS	NOTES
RAM (Random Access Memory)					
HM5116400AJ7	4Mx4 DRAM	Hitachi	CMOS	P: Cell Errors	5V device
4216400-70	4Mx4 DRAM	NEC	CMOS	P: Cell Errors	5V device
D4216400G3-70	4Mx4 DRAM	NEC	CMOS	P: Cell Errors	3.3V device
0116400PT1C-70	4Mx4 DRAM	IBM	CMOS	P: Row and Column Errors	3.3V device
43G9240	4Mx4 DRAM	IBM	CMOS	P: Row and Column Errors	3.3V device
0116400J1C-70	4Mx4 DRAM	IBM	CMOS	P: Cell Errors H: SEU single bit 1.46, Row and column address 3-6 (mode dependent)	5V device
TP0116400AJ3B-70	4Mx4 DRAM	IBM	CMOS	P: Row and Column Errors	-
0116400J1C-70	160 Mbit DRAM Stack	Irvine Sensors	CMOS	P: No SEEs	-
70V25	Dual Port RAM	IDT	CMOS	P: Single Bit Errors	-
628128	SRAM	Hitachi/Elmo	1µ CMOS, with NMOS peripherals	P: Address Errors H: SEU 1.45 (address), 3.38 (bit) SEL > 60	pattern sensitive
Programmable Devices					
SA28C256ARP	EEPROM	SEI	CMOS	H: SEU > 14.9 SEL 14.9-26.2 Hard failure after SEL	-
SA28C256ERPDB	EEPROM	SEI	CMOS/epi	H: SEU 7 (write), 11 (read), > 80 (static) SEL > 90	-
HN58C1001	EEPROM	Hitachi	CMOS/epi	H: SEU 18 (write), > 90 (static/read) SEL > 90	-
E28F016SB	Flash EEPROM	Intel	-	H: SEU 9-11.4 (write) SEL 26.2-29.9	-
UT22VP10	RADPAL	UTMC		H: SEU 37.2 SEL > 90	-
IMP50E10	EPAC	IMP	-	H: SEU < 1.5 SEL 15-26.6	-
A1280	FPGA	Actel	CMOS	P: No SEUs	limited test
AT6002-JC	FPGA	Atmel	0.8µ CMOS, 10µ epi	P: Data SEUs H: SEU 7-8 SEL 11-11.4	-
3090A	FPGA	Xilinx	CMOS	H: SEU 4-7 SEL 3.9-7.88	-
ATT2C04-2	FPGA	AT&T	0.5µ CMOS	H: SEL < 7.88	-
Microprocessors and Peripherals					
MQ80386-25/B	Microprocessor	Intel	CHMOS IV	H: SEU 4-5 (count, reset), 5-6 (lockup) SEL 30-32	microlatch
H30466A-21	Microprocessor	SEI	CHMOS IV (repackaged)	H: SEU 5-6 (count), 3.4-5 (reset), 6-11.4 (lockup) SEL 35-37.5	microlatch
MQ80387-20/B	Math Coprocessor	Intel	CHMOS IV	H: SEU 9-11.4 SEL 32-35	microlatch

DEVICE	FUNCTION	MANUF.	PROCESS	TEST RESULTS	NOTES
Microprocessors and Peripherals (Cont.)					
MQ82380-25/B	Integrated Peripheral	Intel	CHMOS III	H: SEU 3.4 SEL 15-20	destructive SEL and microlatch
M82C59A	Programmable Interrupt Controller	Harris	-	H: SEU 11.4 SEL > 80	-
D8255A-5	Programmable Peripheral Interface	Intel	-	H: SEU < 3.6 (data), 6 (spike) SEL 59.6	current spike
82C54	Timer	Intel	-	H: SEU 9 SEL > 80	-
Voltage/Power Conversion					
ICL7662MTV-4	Voltage Converter	Maxim	-	H: SEU 59.7 SEL > 80	-
MCH2805S	DC-DC Converter	Interpoint	-	H: SEE > 100, No SEEs	-
MDI2680	DC-DC Converter	MDI	-	H: SEE 30	voltage "dropout"
Other					
SP9380	18-Bit DAC	Sipex	-	H: SEU 1.45-3.4 SEL 37.1-59.7	-
QS3384DM	Quickswitch	Quality Semi. Inc.	-	H: SEL 15-18	-
CD4029	Counter	IM	-	P: No Transients	-
HSSR-71110	Power MOSFET Optocoupler	HP	AlGaAs LED; n-chan. power MOSFET	H: SEU > 100 SEL > 100	-
HX2300	SOI Test Metal	Honeywell	RICMOS SOI 4	H: SEU > 120 SEL > 120	-

A. RAM

1. *DRAM*

DRAMs were tested in several modes (dynamic, static, refresh only), with various patterns (0s, 1s, checkerboard) and access methods (byte, page), with no impact to the results. Devices were tested at V_{cc}, and V_{cc}-10% (SEU) and V_{cc}+10% (SEL).

Types of SEUs observed include: *cell* (single bit) errors; *column* or *row* (block) address errors, when a single ion strike induces a partial or full address column or row to be in error; *SEFI* , or Single Event Functional Interrupt; and finally *"stuck" bits*, which cannot be reprogrammed after irradiation. Multiple bit upsets inside a single data structure were not seen.

Figure 1 shows Hitachi and NEC DRAM results, while Figure 2 shows IBM DRAM results. For more information on DRAM test procedure and results, please see LaBel, et al. [1-3].

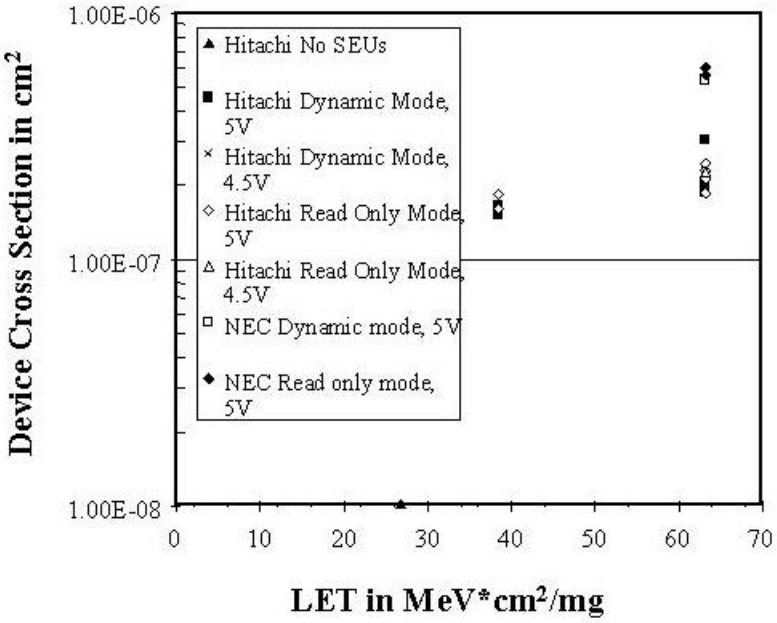

Figure 1 Hitachi, NEC DRAM results

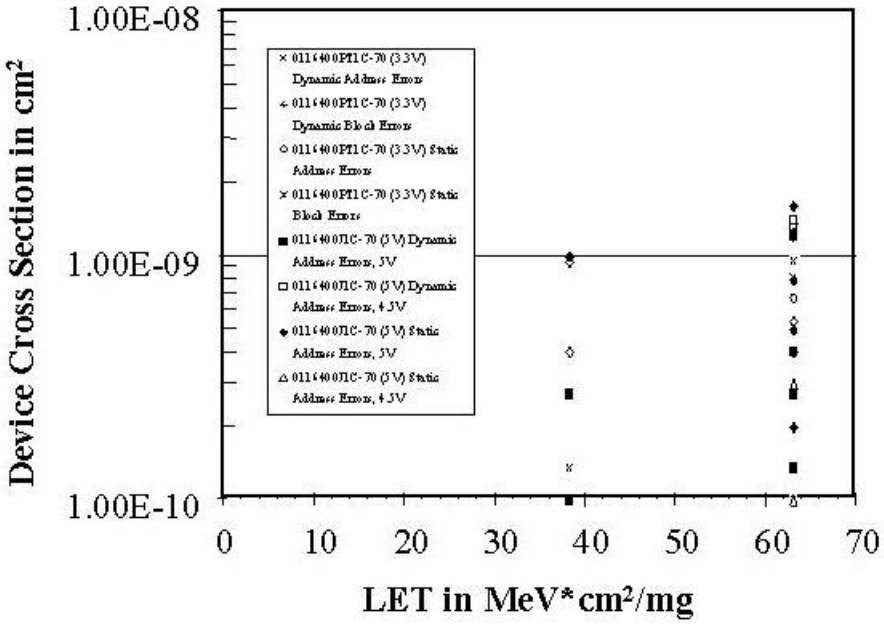

Figure 2 IBM DRAM results

a. HM51116400AJ7 4Mx4 DRAM (Hitachi 5V)

During proton testing, only cell errors were seen, with a cross section of 2E-7 cm*2*/device at 63 MeV.

b. 4216400-70 4Mx4 DRAM (NEC 5V)

During proton testing, only cell errors were seen, with a cross section of 5E-7 cm*2*/device at 63 MeV.

c. D4216400G3-70 4Mx4 DRAM (NEC 3.3V)

During proton testing, only cell errors were seen, with a cross section of 2E-7 cm*2*/device at 63 MeV.

d. 011640OPTIC-70 4Mx4 DRAM (IBM 3.3V)

During proton testing, the cross section for cell errors was < 2E- 9 cm*2*/device at 63 MeV. Block errors were also seen.

e. 43G9240 4Mx4 DRAM (IBM 3.3V)

During proton testing, the cross section for cell errors was 6E-9 cm*2*/device at 63 MeV. Block errors were also seen.

f. 0116400JIC-70 4Mx4 DRAM (IBM 5V)

During proton testing, only cell errors were seen, with a cross section of 2E-7 cm*2*/device at 63 MeV. During heavy ion testing, the LET_{th} for cell errors was ~ 3, and for block errors ~ 5, with a maximum measured cross section of 7E-2 cm*2*/device at an LET of 50. SEL was not seen, up to an LET of 50.

g. TP0116400AJ3B-70 4Mx4 DRAM (IBM)

During proton testing, the cross section for cell errors was 6E-9 cm*2*/device at 63 MeV. One block error was also seen.

h. 0116400JIC-70 160 Mbit DRAM Stack (IBM 5V)

During proton testing, no SEUs were seen up to an energy of 197 MeV, although they were expected based on single chip tests.

2. *70V25 Dual-Port SRAM*

This device was tested dynamically - the DUT was written to/read from simultaneously during irradiation - using a toggle input. During proton testing, the device experienced single-bit errors beginning at an energy of 26.6 MeV, but no multiple-bit errors up to the maximum test energy of 63 MeV. Previous heavy-ion testing found SEU LET_{th} to be < 3.46, with a maximum cross section of 5E-7 cm*2*/bit, and some multiple bit errors. No latchup was seen for LETs up to 80.

3. *628128 SRAM*

A static mode test was performed on the 628128 SRAM. The DUT was loaded with all 0s or all 1s, and then checked for addresses in error. During heavy ion testing, the LET_{th} for SEUwas ~ 1.4. SEL was not observed, up to an LET of 52.5. During proton testing, pattern sensitivity was discovered; the device was approximately twice as sensitive to SEU with the all 1s pattern, than with the all 0s pattern.

B. Programmable Devices

1. *EEPROMs*

EEPROMs were tested using a checkerboard pattern in the following modes:

Static - device loaded prior to beam, irradiated to a known fluence, then read back for errors

Read only - device loaded prior to beam and read continuously during irradiation.

Write in byte mode - device programmed byte-by-byte during irradiation, then verified post-irradiation

Write in page mode - device programmed page-by-page during irradiation, then verified post-irradiation

The number of bytes in error was monitored. Figure 3 shows results for several EEPROMs.[4]

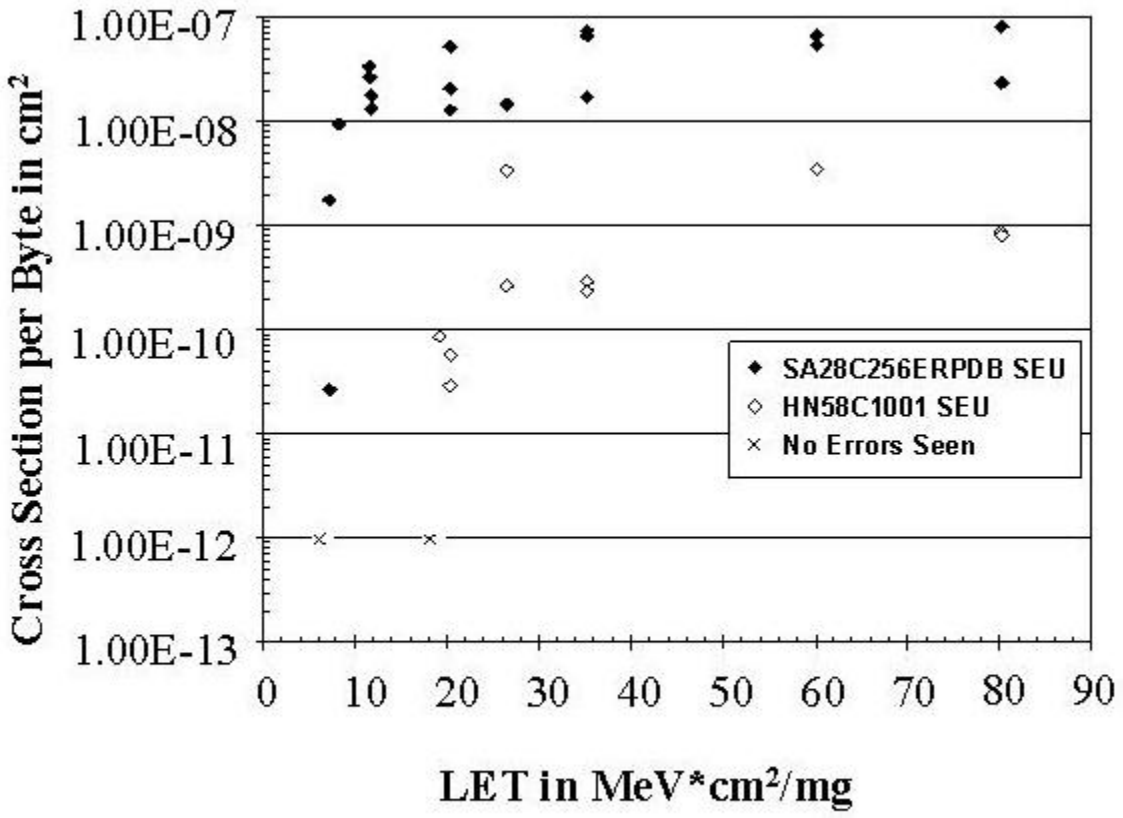

Figure 3 EEPROM SEU Data

a. SA28C256ARP EEPROM

Nominal V_{cc} for this device (standby mode) is 5V/16-25mA. SEL current was set to 80mA. No SEUs were seen in any mode of operation up to maximum tested LET of 14.9. SEL LET_{th} is between 14.9 and 26.2. Both test samples failed with device I_{cc} exceeding 1.5A after experiencing SEL.

b. SA28C256ERPDB EEPROM

Nominal V_{cc} for this device (standby mode) is 5V/6-22mA . SEL current was set to 80mA. No SEUs were seen in static mode of operation up to maximum tested LET of 80. Sporadic SEUs (no statistical data) were seen on read mode operations starting at an LET of 11 with a maximum device byte cross-section of < 1E-6 cm^2. est results for the write byte and write page modes were equivalent. LET_{th} was 7. LET_{th} for SEL is > 90.

c. HN58C1001 EEPROM

Nominal V_{cc}/I_{cc} for this device (standby/operating mode) is 5V/5-9mA . SEL current was set to 50mA. No SEUs were seen in static or read mode of operation up to the maximum tested LET of 80. Test results for the write byte and write page modes were equivalent. LET_{th} was 18. SEL LET_{th} is > 90.

2. *E28F016SB 16 Mbit (1Mx16)Flash EEPROM*

Nominal V_{cc}/I_{cc} for this device (standby/operating mode) is 5V/1-5mA . SEL current was set at 40mA. The device was tested with a checkerboard pattern in three modes:

Static or cell storage - device loaded prior to beam, irradiated to a known fluence, then read back for errors

Read only - device loaded prior to beam, and read continuously during irradiation.

Write only - device programmed during irradiation, then verified post-irradiation.

SEL was observed for all test modes starting at LETs of between 26.2 and 29.9 (first observed), but not on every test run at LETs %29.9, hence cross-section at max tested LET (59.9) is < 1E-6cm*2* per device. Control SEUs (incomplete writes, or incorrect pointer leading to blocks of errors) were observed on write mode tests staring at LETs between 9 and 11.4. No other data SEUs were observed for write mode. Sporadic data errors (i.e., bitflips) were seen on only two other test runs (1 on read mode, 1 on static mode) out of more than 20. With such few examples occurring, no statistical data is available. However, data errors may be attributable to test setup noise and may not be directly related to the ion beam. The cell storage mechanism is not expected to upset. No other SEUs were noted on read or static mode. [5]

3. *UT22VP10 RADPAL*

During testing, the UT22VP10 was programmed with some typical logic circuits. The test ran in active mode, with a clock rate of 1 MHz. The device was tested with V_{cc} of both 5V and 4.5V. SEUs were observed, starting at an LET of 37.2 MeV*cm*2*/mg. The cross section was negligibly higher when device V_{cc} was reduced from 5V to 4.5V. SEL was not observed on any test run, up to a maximum tested LET of 90.[6]

4. *IMP50E10 EPAC*

The 50E10 is a user-configurable analog device consisting of op-amps with EEPROM for configuration. For this test, it was programmed with several op-amps in a summing configuration. Device input was a sawtooth at 2kHz. SEUs were observed at the lowest tested LET of 1.45. SEL LET_{th} was between 15-26.6.

5. *A1280 FPGA*

The device was programmed with typical combinatorial logic and shift registers, and tested with a toggle pattern input, at a frequency of 1MHz. During proton testing, no SEEs were observed, at an energy of 197 MeV.

6. *AT6002-JC FPGA*

For testing, this FPGA was programmed to utilize 1024 of 2000 usable gates, and 8k of 64k of Configuration RAM. While being irradiated, a 100kHz clock was fed through a 1024 stage shift register. The DUT was monitored for data and reconfiguration errors. The LET_{th} for both data and reconfiguration errors was 7-8. The LET_{th} for SEL was 11-11.4. During SEL, I_{cc} jumped from 60mA to 200-232mA; all SELs were recoverable with power resets. [7]

7. *3090A FPGA*

For testing, the DUT was programmed with 16 8-bit counters, (8 on each bus), 4 8-bit shift registers, and 8 8-bit flip-flops. 166 of 320 CLB units were used, for 51% utilization. Clock speed was 1 MHZ. The DUT was monitored for data and reconfiguration errors. Threshold for reconfiguration errors is between LET 4.1-7.9, and for data errors is between 9.6-11.4. Figure 4 shows test results. SEL LET_{th} is ~7.9. During SEL, I_{cc} jumped from 10mA to 20mA; all SELs were recoverable with power resets, until device failure occurred with I_{cc} exceeding 70mA.

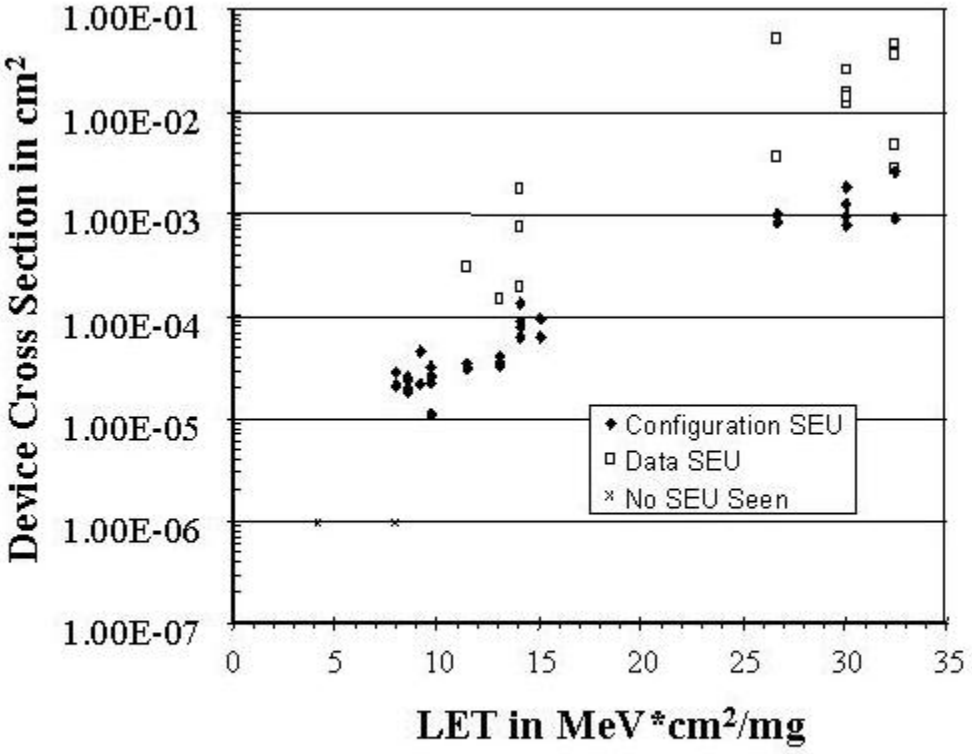

Figure 4 Xilinx 3090A FPGA

8. *ATT2C04-2 FPGA*

For testing, this FPGA was programmed with a 4 structures, each with a 2x4 FIFO configuration, with 1024 of 6400 bites of configuration RAM utilized. Clock speed was 10 MHZ. The DUT was monitored for data and reconfiguration errors. During limited testing, no data errors were seen. Threshold for both reconfiguration errors and SEL is < 7.88. During SEL, I_{cc} went from 25mA to 189-300mA; device failure ensued due to a hole burnt into the substrate.

C. Voltage/Power Conversion

1. *ICL7662MTV-4 Voltage Converter*

This voltage controller was tested with V_{cc} of 15V, 21V, 28V, and 35V. DUT output was monitored for glitches and long errors. Errors were seen only with V_{cc} of 15V. With 15V V_{cc}, the device was tested over the LET range of 59.7-80; SEUs were seen at all LETs, but SEL was not observed.

2. *MCH2805S DC-DC Converter*

The MCH2805S is a DC-DC power converter with 28V input, and a single output of 5V, which was loaded with a 33W/2W resistor for the test. During testing, input voltage was varied by % 7V. The device was monitored for glitches and "long errors", defined as variations in the voltage output by greater than 0.5V. No single event effects of any kind were observed, up to an LET of 82.7.

3. *MDI2680 DC-DC Converter*

The 2680 was tested to determine the effectiveness of additional RC circuitry on an LM139 op-amp used in the MDI 2690 type converters (MDI proprietary) to fix a single event effect observed in other MDI: the converter output would drop from +5V to 0V for brief intervals (microseconds). Heavy ion testing revealed an LET_{th} for the dropout condition of 30. Power cycling was required for the device to recover.[8]

D. Microprocessors and Peripherals

1. *80386 Test Set*

The 80386, 80387, and 82380 devices were tested using a single-board computer. Custom software exercised the devices by performing memory accesses, addressing, data transfers, and numerical calculations. External clock speed is 16 MHZ.

Three types of SEU were monitored: *Count* - the device fails to write to a test address, or it performs a memory transfer or calculation incorrectly; *Reset* - the device locks up, I_{cc} remains at typical operating level, and the condition is cleared by a reset signal (power is not cycled). Most likely the SEU, either alone or through propagation to the system, places the test device or a peripheral into an unknown state; and *Lockup* - the device locks up, I_{cc} drops to a current indicative of standby operating mode, and the condition requires a power reset to recover. Most likely the SEU places the test device or a peripheral into an undefined, test, or standby mode. Test runs were halted upon lockup.[9]

a. MQ80386-25/B Microprocessor

The LET_{th} (threshold) is between 4-5 for count and reset SEUs, and between 5-6 for lockup SEUs. During lockup, the device current dropped from normal operating current of 134mA to ~100mA; the device is suspected to be entering a standby mode. Traditional SEL was not seen on any test run. However, microlatch was observed, with an LET_{th} between 30 and 32. A two-minute dwell test was performed following a microlatch; the device recovered fully following a power reset. Data for the 80386 is presented in Figure 5.

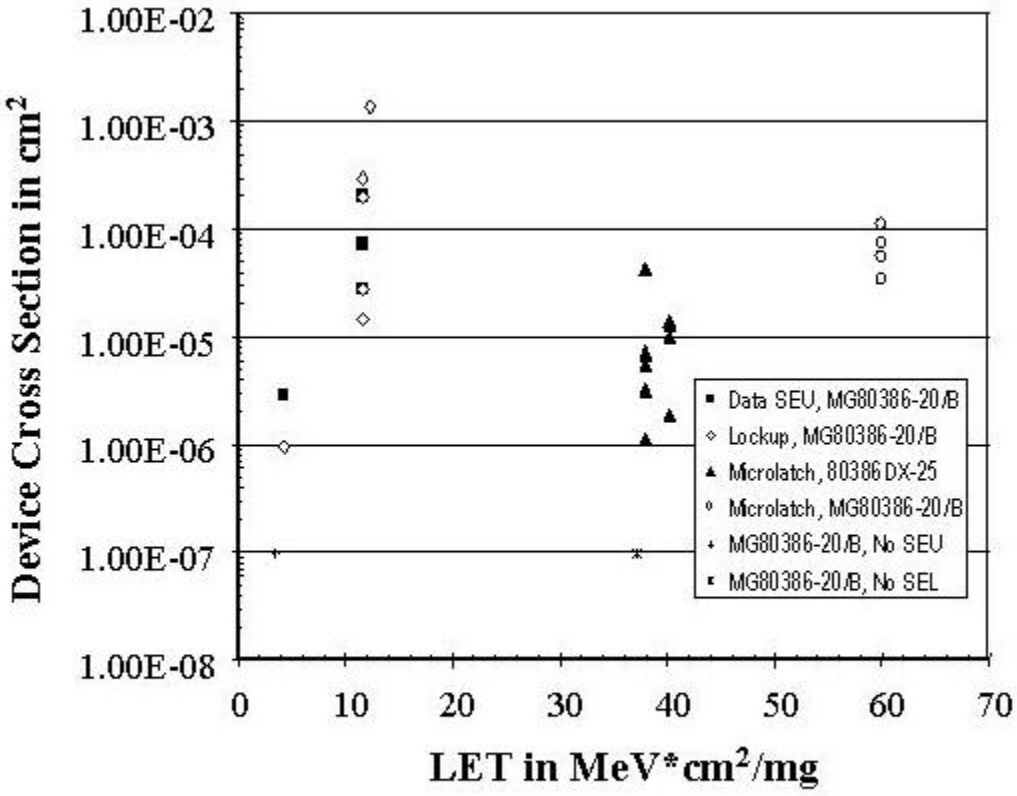

Figure 5 80386 Data

b. H30466A-21 Microprocessor

LET_{th} is between 5-6 for count SEUs, between 3.4-5 for reset SEUs, and between 6-11.4 for lockup SEUs. Traditional SEL was not seen on any test run. However, microlatch was observed, with LET_{th} between 35-37.5. A 15-minute dwell test was performed, with the device in a microlatch state; the device recovered fully following a power reset.

c. *MQ80387-20/B Math Coprocessor*

The LET_{th} is between 9-11.4. Only count and reset SEUs were seen; lockup SEUs were not. LET_{th} for microlatch was between 32 and 35. During a microlatch, the current jumped from a typical 60mA to between 154-223mA. The device remained functional during a microlatch; upon a reset signal, the device would functionally recover, while the current remained at the higher microlatch level. A power reset brought the current back to normal levels. Additionally, a 15-minute dwell test was performed, with the

device in this microlatch state. The device recovered fully following a power reset. Traditional SEL wasnot observed.

d. *MQ82380-25/B Integrated Peripheral*

LET_{th} for reset SEUs was ~ 3.4. Count and lockup SEUs were not observed. Figure 6 displays 82380 data. Both microlatch and traditional SEL were observed, with an LET_{th} between 15-20. During several test runs, the device experienced a traditional SEL (with a device current of 387mA, exceeding the specified maximum of 375mA), which was cleared entirely by a software reset. It is suspected that the device actually experienced an SEU which placed it in a test mode.

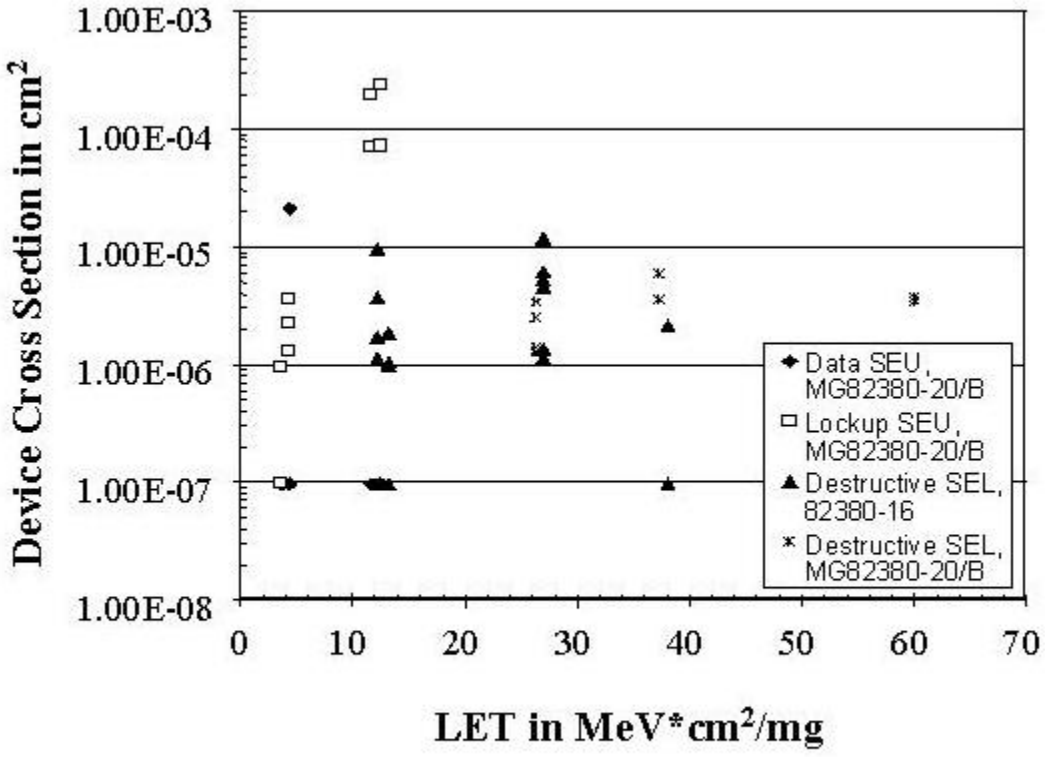

Figure 6 82380 Data

82380 SEL testing was complicated by the fact that the 82380 and 80386 currents were coupled; whenever the 82380 experienced SEL, the 80386 showed a corresponding increase in current, most likely due to a bus contention. Despite this coupling, a two-minute dwell test was performed. The 82380 and 80386 both recovered fully, following a power reset.

2. *M82C59A Programmable Interrupt Controller*

This device was tested using a 1 MHZ clock; interrupt mismatch between the DUT and a reference device was counted as an error. SEUs were observed at the lowest tested LET of 11.4, but not on all test runs at higher LETs. SEL was not observed up to an LET of 80. Figure 7 displays data for this, the D8255A-5, and the 82C54.

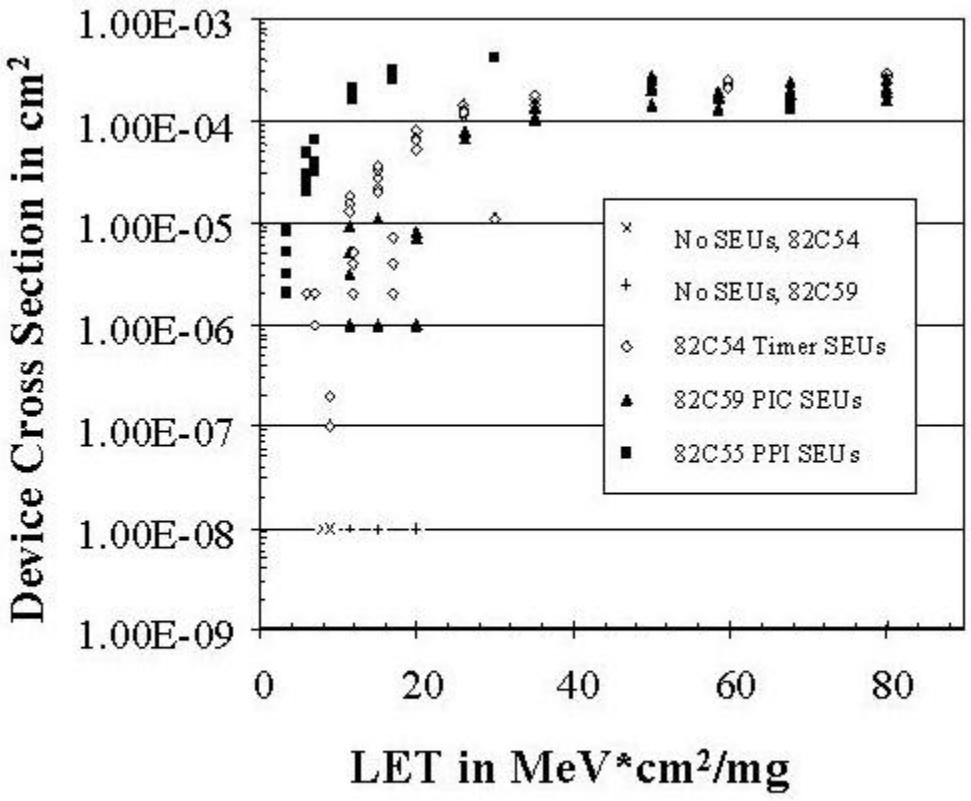

Figure 7 Microprocessor Peripherals

3. *D8255A-5 Programmable Peripheral Interface*

An SEU for this device was defined as a mismatch in a 9-bit output, between the DUT and a reference device. The DUT experienced SEUs at the lowest LET tested of 3.6, along with current spikes, starting at an LET of 6. During the current spikes, I_{cc} jumps from the typical level of 42mA to 100mA orabove. SEL was observed on only two test runs at an LET of 59.6, but not at higher LETs; the events may actually have been two spikes in a row. Figure 7 displays data for this, the M82C59A, and the 82C54.

4. *82C54 Timer*

This device was tested using a 1 MHZ clock; a mismatch between the DUT and a reference device was counted as an error. LET_{th} for SEUs was ~ 9. SEL was not observed up to the maximum tested LET of 80. Figure 7 displays data for this, the M82C59A, and the D8255A-5.

E. Other

1. *SP9380 18-Bit DAC*

This device was tested at 16 kHz, with a resolution of 13½ out of 18 bits (~ 1 mV). A mismatch between the DUT and a reference device was counted as an error. LET_{th} was between 1.45-3.4 for SEU, and between 37.1-59.7 for SEL. A single destructive event was observed at an LET of 59.7, following which the device was nonfunctional.

2. *QS3384DM Quickswitch*

This 10-bit bus switch was tested at 1 MHZ, with a checkerboard input. No SEUs were seen, but SEL LET_{th} was between 15-18.

3. *CD4029 Counter*

The CD4029 is an up-down counter. It was tested with a 6.6 MHZ clock input, and monitored for both glitches and bitflips. No single event effects were seen, at an energy of 63 MeV.

4. *HSSR-71110 Power MOSFET Optocoupler*

During testing, this DUT was operated as a solid-state relay. The device was monitored for any change of state. No single event effects of any kind were seen, up to an LET of 100.

5. *HX2300 SOI Test Metal*

The Test Metal was configured with 200 stage shift register each of JK, D, and RS flip-flops, and with test patterns of all 0's, all 1's, and checkerboard. The device was tested in both static (device pre-loaded, then irradiated, then checked for errors post- beam) and dynamic (continuous R-W at a 1 MHZ frequency) mode. Testing was performed with device V_{cc} of 5V and 4.5V.

During heavy ion testing, no single event effects were seen, up to an LET of 120. This process is a true RH process. SEU rate prediction for a device fabricated on this process is statistically zero upsets per day (no orbit dependence). This process appears to be as hard as any CMOS/SOS process we have tested.

IV. Recommendations and Conclusions

Following proton and/or heavy ion testing, devices are categorized into one of four categories for recommendation to the flight project of interest:

Category 1 Recommended for usage in all spaceflight applications; relatively hard or immune to SEEs

Category 2 Recommended for usage in spaceflight applications; somewhat susceptible to SEEs, and may require some SEE mitigation

Category 3 Recommended for usage in some spaceflight applications; very susceptible to SEEs, requires extensive SEE mitigation or SEL recovery mode

Category 4 Not recommended for use in any spaceflight applications; destructive conditions were seen at low LETs

The devices described in this paper are categorized as follows in Table 3:

Table 3 *Device Recommendations*

Category 1	Category 2	Category 3	Category 4
RAM			
0116400J1C (stack);	0116400J1C (single chip); TP011640AJ3B-70; 70V25; 628128	HM5116400; 4216400-70; D4216400G3; 011640OPT1C; 43G9240	-
Programmable Devices			
UT22VP10; A1280	SA28C256ERPDB; HN58C1001	Category 2/3: E28F016SB	SA28C256ARP; IMP50E10; 3090A; ATT2C04-2; Category 3/4: AT6002-JC
Microprocessors, Peripherals			
-	M82C59A; 82C54	MQ80386-25B; H30466A-21; MQ80387-20B; MQ82380-25B; D8255A-5	-
Voltage/Power Devices			
ICL7662MTV; MCH2805S; MDI2680	-	-	-
Other Devices			
CD4029; HSSR-71110; HX2300	-	SP9380; QS3384DM	

V. Acknowledgments

The authors would like to acknowledge the participating Goddard programs, namely NASA Headquarters/Code Q, Hubble Space Telescope, Landsat-7, and others. Special thanks to the Naval Research Laboratory, BNL, UCD, and IUCF facilities.

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