Compendium of Recent Total Ionizing Dose Results for Candidate Spacecraft Electronics for NASA

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Abstract—Radiation Effects testing on a variety of candidate spacecraft electronics to total ionizing dose is studied. Devices tested include digital, analog, mixed signal, and hybrid devices.

Index Terms- Total Ionizing Dose.

I. INTRODUCTION

In order to meet the demands of reduced cost, higher performance and more rapid delivery schedules imposed by the space flight community, commercial and emerging technology devices have assumed a prominent role in meeting these needs. Thus, the importance of ground based testing for the effects of total ionizing dose (TID) to qualify such devices for flight is paramount. The novel ways in which some of these devices are used also highlights the need for application specific testing to ensure their proper operation and ability to meet mission goals.

The test results presented here were gathered to establish the sensitivity of the devices selected as candidate spacecraft electronics to TID. This testing serves to determine the appropriateness of a candidate device which may be used in space applications. For single event effects (SEE) results, see a companion paper submitted to the 2008 IEEE NSREC Radiation Effects Data Workshop entitled: "Compendium of Recent Single Event Effects Results for Candidate Spacecraft Electronics for NASA" by M. O'Bryan, et al. [1]

II. Test Techniques and Setup

A. *Test Facilities – TID*

TID testing was performed using a Co-60 source at the Goddard Space Flight Center Radiation Effects Facility (GSFC REF), Table I. The source is capable of delivering a dose rate from sub-mrad(Si)/s, to in excess of 30 rads(Si)/s, with dosimetry being performed using a chamber probe.

B. *Test Methods*

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages.

1) *TID Testing*

TID testing was performed to the MIL-STD-883 1019.7 test method [2].

III. Test Results Overview

Abbreviations for principal investigators (PIs) are listed in Table I. Abbreviations and conventions are listed in Table II. Table III provides a summary of TID test results. This paper is a summary of results. Please note that these test results can depend on operational conditions. Complete test reports are available online at http://radhome.gsfc.nasa.gov [3]. Degradation is defined as device parameter(s) exceeding specification limit(s) or functional abnormalities noted.

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TABLE I: LIST OF PRINCIPAL INVESTIGATORS

Abbreviation	Principal Investigator (PI)
SB	Stephen Buchner
MC	Martin Carts
TO	Timothy Oldham
SM	Susan Mackey
CP	Christian Poivey
AS	Anthony Sanders

TABLE II: ACRONYM DEFINITION

ADC = ANALOG TO DIGITAL CONVERTER
ASIC = APPLICATION SPECIFIC INTEGRATED CIRCUIT
CCD = CHARGE COUPLED DEVICE
CMOS = COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
DAC = DIGITAL TO ANALOG CONVERTER
DNL = DIFFERENTIAL NON-LINEARITY
FET = FIELD EFFECT TRANSISTOR
IB = BIAS CURRENT
IC = COLLECTOR CURRENT
IF = FORWARD CURRENT
IOS = OFFSET CURRENT
ISTDBY = STANDBY CURRENT
LDC = LOT DATE CODE
LED = LIGHT EMITTING DIODE
ICC = POWER SUPPLY CURRENT
MEV = MEGA ELECTRON VOLT
N/A = NOT APPLICABLE
OP AMP = OPERATIONAL AMPLIFIER
P/CM2 = PROTONS/CM2
PI = PRINCIPAL INVESTIGATOR
PT = PHOTO TRANSISTOR
TID = TOTAL IONIZING DOSE
VOL = OUTPUT SATURATION VOLTAGE
VOUT = OUTPUT VOLTAGE
VCE = COLLECTOR EMITTER VOLTAGE

TABLE III: SUMMARY OF TID TEST RESULTS

Part Number	Manufacturer	LDC	Technology	Device Function	Facility Date/P.I *(Co-60 source unless otherwise noted).*	Summary of Results [Test Report]	Dose rate (rads(Si)/s)	Degradation Level (krads(Si))
Data Converters								
AD7821	Analog Devices	0449B	CMOS	8-bit ADC	GSFC07FEB/AS	Conversion errors began after 10 krad; slight drop (approx 2% per 5k dose) in supply current.	20	~10
AD5334	Analog Devices	535	CMOS	8-bit DAC	GSFC07FEB/AS	Experienced current instability after 5 krad(Si).	20	~5
AFL2828SX/CH	Intl Rectifier	533	Hybrid	DC/DC Converter	GSFC07JUN/SM	Degradation noted on Vout but within specification.	10	>30
SMSA2815S	Interport	615	Hybrid	DC/DC Converter	GSFC07SEPT/SB	No changes in any of the parameters up to 50 krad(Si).	20	>50
SMSA2815S	Interport	651	Hybrid	DC/DC Converter	GSFC07SEPT/SB	No changes in any of the parameters up to 50 krad(Si).	20	>50
Linear – Amplifiers								
RM124	National Semiconductor	Wafer 01	Bipolar	Op Amp	GSFC07MAR/SB	This part was exposed to 100 krad(Si) and remained within specification.	1.5	>100
AD713S	Analog Devices	708	BiFET	Quad Op Amp	GSFC07SEPT/SB	Positive input current exceeded specified max at 20 krad(Si). Input offset voltage exceeded specifications at 10 krad(Si). Other parameters remained within specification.	20	~10

Part Number	Manufacturer	LDC	Technology	Device Function	Facility Date/P.I *(Co-60 source unless otherwise noted).*	Summary of Results [Test Report]	Dose rate (rads(Si)/s)	Degradation Level (krads(Si))
Logic Devices								
54AC273	National Semiconductor	0502A	CMOS	Octal-D	GSFC07DEC/SB	Application-specific test to determine shift in threshold voltage. At 10 krad(Si) the shift was approximately 30 mV.	1.5	N/A
Memory								
HY27UF084G2M	Hynix	636A	CMOS	NAND Flash 4Gb	GSFC07DEC/TO	Failed between 30-75 krads.	25	30-75
MT29F4G08AAAWP	Micron	628	CMOS	NAND Flash 4Gb	GSFC07DEC/TO	Failed 50-200 krads.	25	>50
K9F4G08U0A	Samsung	625	CMOS	NAND Flash 4Gb	GSFC07DEC/TO	Failed 100-200 krads.	25	>100
K9K4G08U0A	Samsung	622	CMOS	NAND Flash 4Gb	GSFC07JAN/TO	Zero bias test-failed 400-700 krads.	25	>400
MR2A16ATS35CUOYAN	Freescale	629	MRAM	NAND MRAM	GSFC07/OCT/TO	Failed 90-110 krads.	25	>90
FPGAs								
XC4VFX60	Xilinx	609	FPGA	FPGA	GSFC07JUL/CP	No degradation up to 240 krads.	0.3-0.6	>241
Voltage References, Regulators & Comparators								
AD549SH/883	Analog Devices	0630B	CMOS	Op Amp	GSFC07JAN/AS	All parameters are within specification up to 30 krad(Si).	20	>30
MAX997	Maxim	531	CMOS	Voltage Comparator	GSFC07FEB/AS	All parameters are within specification; the input offset voltage was not measured.	20	>30
Miscellaneous								
SR-ESAPMOS4/RAD	Natl Micro Research Ctr	0608 LaRC's lot, wafer #2	CMOS	Dosimeters on SET-1	GSFC07APR/MX	Dosimeters were calibrated using the GSFC Co-60 source.	0.1	100
SA8016	Philips	C045132	BiCMOS	Fractional N Synthesizer	GSFC07AUG/MC	No change over 30 Krad(Si).	0.0085	>25
MIC4423	Micrel	513	BiCMOS	MOSFET Driver	GSFC07FEB/AS	All parameters are within specification up to 30 krad(Si).	20	>30
OMH3075S	Optek Technologies	M0551	CMOS	Hall Effect Sensor	GSFC07JAN/AS	All parameters are within specification up to 40 krad(Si).	20	40
AD654	Analog Devices	451	CMOS	Voltage to frequency converter	GSFC07APR/SB	Only parameters to show any change were input voltage required to produce an output frequency of 1 Hz and output frequency when input voltage is 0V. Application specific test setup so comparison with manufacturer's data sheet difficult.	20	15-20

IV. Test Results and Discussion

As in our past workshop compendia of GSFC test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [3] describing in further detail, test method, TID conditions/parameters, test results, and graphs of data.

1) *Philips, SA8016, Fractional N Synthesizer*

This study was undertaken to determine the TID hardness of the Phillips SA8016DH 2.5 GHz low voltage fractional-N frequency synthesizer. The device features a BiCMOS process technology (Phillips QUBiC2), single supply operation from 2.7 to 5 Vdc, programmable reference and main dividers, a phase comparator, charge pump, and fractional division frequency spur reduction. At the sponsoring application's supply voltage of 3 Vdc it dissipates approximately 33 mW. When integrated with a low pass filter, a VCO and a 3-wire serial programming source (48 bit configuration string) it functions as a tunable phase-continuous frequency synthesizer. Fig. 1 is a block diagram of this device.

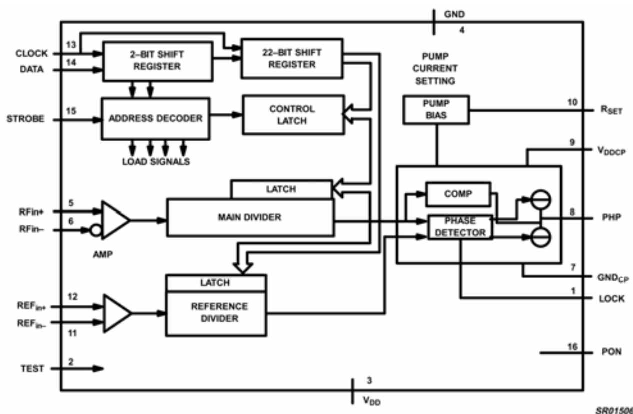

Figure 1. Block Diagram of SA8016 Low Voltage Fractional-N Synthesizer

TID testing was performed at the GSFC REF according to MIL-STD 1019.7 Enhanced Low Dose Rate Sensitivity (ELDRS) criteria of 10 mrad-Si/sec because this is a mixed, bipolar and CMOS device technology. Actual dose rate was 8.5 mrad-Si/sec. The device was operated in an open-loop state and at nominal room temperature during irradiation. (Given the low internal power dissipation the device die temperature is assumed to be ambient, 25C.) A step irradiation was performed with certain measurements performed periodically during irradiation and other measurements, not amenable to in-situ collection, taken at steps of, roughly, 0, 5, 10, 15 and 25 krad-Si. Measurements of power draw and divider/detector responsiveness in an open-loop configuration were taken periodically (generally every 15 minutes, about every 5 rad). Actual closed-loop functionality necessarily involved a physically near-by VCO which was not a radiation-characterized component and so was measured at the above intervals when the irradiation was paused.

One anomaly was noted during testing: Twice the in-situ divider/phase detector functionality testing of all four parts failed during irradiation. The first time power was cycled and the parts regained functionality. The second time the parts were purposefully not power cycled, but merely the configuration string (the 48 bits of programming for the two dividers, along with some other functions) was re-sent to the DUTs. All four parts regained functionality with this re-configuration. No correlation to radiation or operation (e.g. the time or dose since configuration) could be found. An intense period of irradiator shutter activity (during TID facility safety verification testing) did correlate to both of these events but subsequent periods of high shutter activity did not produce any need for reconfiguration. Given that these functional lapses always happened to all DUTs at the same time, and that they were not replicable, and given that in the sponsoring application the device would be reconfigured before every communication (thus making any such effect invisible to the application) it was decided that the best and most likely conclusion is that these were due to the operation of the Co-60 facility and not DUT-related.

2) *Micrel, MIC4423, MOSFET Driver*

The MIC4423 is a dual 3A-Peak Low-Side MOSFET Driver by Micrel. The part was tested to a total dose of 30 krad(Si) at a dose rate of 20 mrad(Si)/s. All devices passed all parametric tests up to a total dose of 30 krad(Si). Figs. 2 and 3 show the Output resistance HI State and LO State. The maximum output allowed was 5 ohms. Data for the average of 5 parts as well as for the control device are included. The error bars show the standard deviation from the measurements.

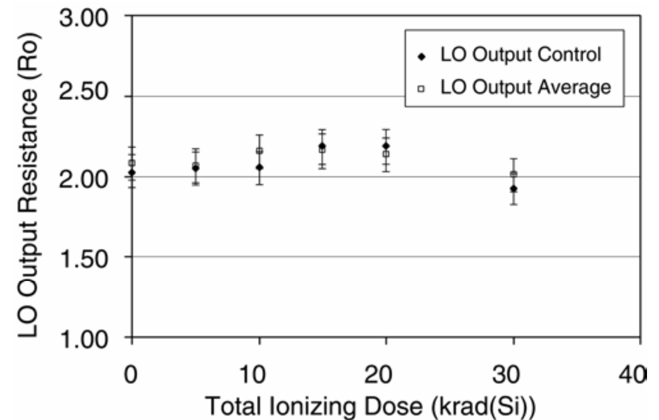

Figure 2. LO Output Resistance

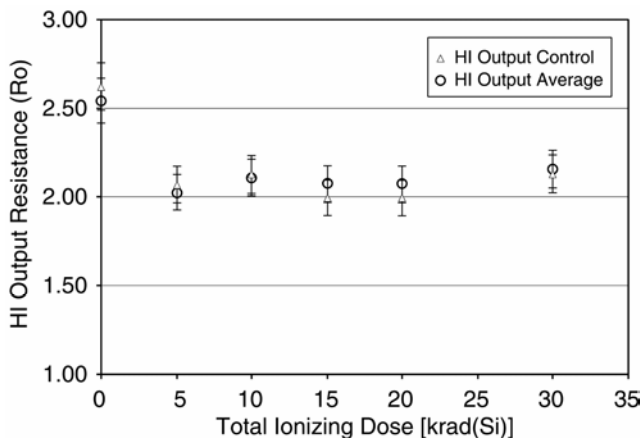

Figure 3. HI Output Resistance

3) Analog Devices, AD654, Voltage to Frequency Converter

The AD654 is a voltage-to-frequency converter manufactured by Analog Devices. By varying the input voltage from –Vs (negative supply) to +Vs-4V, the output varies from 0 Hz to 500 kHz. Various parameters, including output rise and fall times, input currents, and voltages required to produce various output frequencies, were measured as a function of total dose. The parameters showed relatively little change with total dose. Fig. 4 is a plot of output frequency for an input of 7.5 Volts.

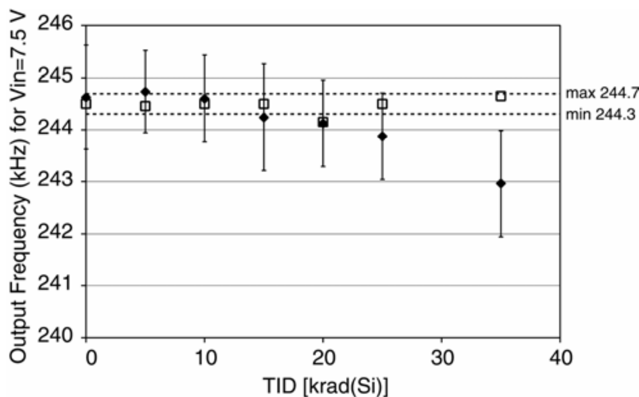

Figure 4. Average output frequency for eight parts as a function of total ionizing dose for an input voltage of 7.5 V (diamonds). The squares are the average measurements for two control devices.

4) Xilinx, XC4VFX60, FPGA

TID irradiations were performed on 4 samples with NASA-GSFC Co-60 source. 4 Parts of date code 0629 were irradiated up to a total dose level of 241 krad-Si at a dose rate ranging from 0.3 to 0.6 krad-Si/s. After irradiation parts were submitted to a one-week annealing at room temperature.

FPGA test vehicle includes two processor nodes and a large shift register made of 8 chains of 2000 flip-flops [4, 5]. Parts were dynamically biased during irradiation with 1 MHz clock and nominal power supplies (core: 1.2V, Aux: 2.5V, I/O: 3.3V).

Before irradiation and after each irradiation step, a full functional test was performed at high speed with NASA REAG high-speed digital tester (HSDT) on the 4 irradiated parts and one control part. Power PCs were tested at a 250 MHz clock with a multi-interrupt program [5]. Shift registers were tested at a clock speed of 125 MHz. In addition to functional test, core, aux, and I/O power supply currents were measured.

No degradation of functional performances or electrical parameters was observed up to the maximum tested dose of 241 Krad-Si and one week of room temperature annealing. Fig. 5 shows the measurements of power supply current versus total dose on the 4 irradiated parts.

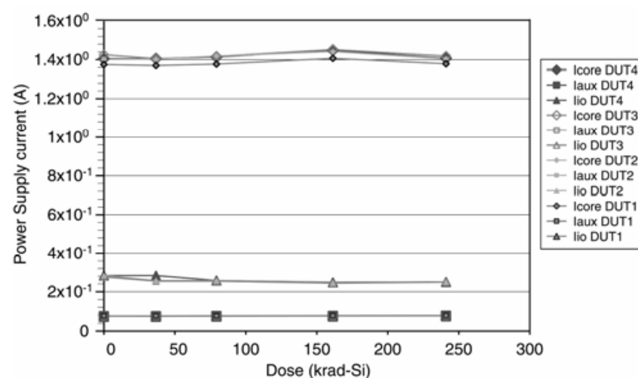

Figure 5: Power Supply Currents Versus Total Dose

5) Freescale, MR2A16ATS35CUOYAN, MRAM

The Freescale MR2A16A uses a magnetic tunnel junction (MTJ) as the storage element. There are two magnetic layers, where the magnetic spins are polarized either parallel or anti-parallel, which causes a change in the electrical resistance of the device (see Fig. 6). This is the so-called GMR (giant magneto-resistive) effect, where the difference in resistance indicates the difference between a zero and a one. (Devices where information is stored in the magnetic spins, rather than by charge storage, are sometimes referred to as spintronic devices.) In this test, there were no errors in any DUT up to, and including, 90 krads (SiO_2). The first errors were observed at 100 krads (SiO_2), with many more errors at 110 krads (SiO_2). The first DUT to fail was at 100 krads (SiO_2), and all had failed at 110 krads (SiO_2). The failures are believed to be due to radiation damage to the CMOS peripheral control logic, rather than to the MTJ, itself. When errors were detected in the initial read operation after the exposure, we usually tried to reset the errors. But activating the control logic for this purpose increased the number of errors significantly.

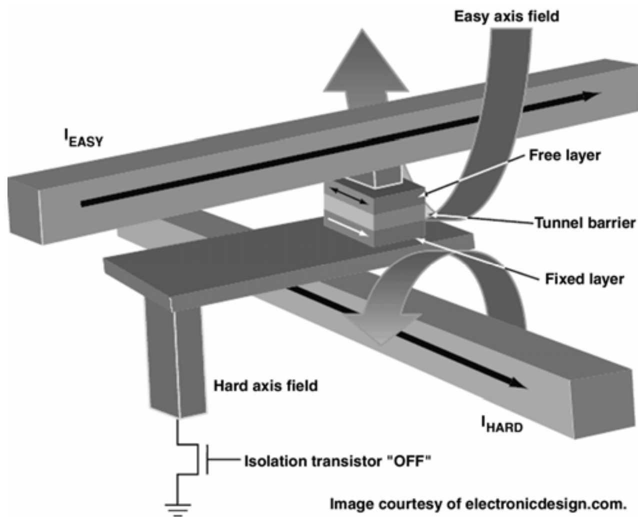

Figure 6. Schematic of magnetic storage element, with two magnetic layers, where spins are either parallel (low resistance) or anti-parallel (high resistance).

V. Summary

We have presented data from recent TID and proton-induced damage tests on a variety of primarily commercial devices. It is the authors' recommendation that this data be used with caution. We also highly recommend lot and application specific testing be performed on any suspect or commercial device.

VI. Acknowledgment

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VII. References

[1] M. O'Bryan, et al., Compendium of Recent Single Event Effects Results for Candidate Spacecraft Electronics for NASA" submitted to the 2008 IEEE NSREC Radiation Effects Data Workshop.

[2] Department of Defense "Test Method sTANDARD Microcircuits," MIL-STD-883 Test Method 1019.7 Ionizing radiation (total dose) test procedure, September 30, 2006, http:/www.dscc.dla.mil/downloads/MIL-STD-883/std883.pdf

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[4] C. Poivey, M. Berg, M. Friendlich, Hak Kim, D. Petrick, S. Stansberry, K. A. LaBel, C. Seidleck, A. Phan, and T. Irwin, “Single Event Effects (SEE) Response of Embedded Power PCs in a Xilinx Virtex-4 FPGA for a Space Application,” Presented at RADECS 2007.

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