Virtex-II Pro PowerPC SEE Characterization
Test Methods and Results

Session L: Birds of a Feather

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Introduction

\begin{itemize}
  \item Prior Xilinx Virtex-II Pro SEE testing
    \begin{itemize}
      \item Memec COTS board
      \item Heavy ions at TAMU and MSU
      \item Focus: PowerPC, MGTs, and SEL
    \end{itemize}
  \item Current Xilinx Virtex-II Pro SEE testing
    \begin{itemize}
      \item Xilinx Radiation Test Consortium board
      \item Protons at IUCF
      \item Focus: PowerPC(s)
    \end{itemize}
\end{itemize}
XRTC Board – Daughter Card

- Xilinx Virtex-II Pro
  - XQR2VP40-FF1152
  - Dual PowerPCs
  - 15,868,256 configuration bits
- External interfaces
  - Platform flash devices
  - JTAG/SelectMAP
  - CPU debug headers
  - RS-232
  - 2 300-pin Teradyne connectors
  - SMPX MGTs
- Isolated power lugs
- Available with socket

XRTC Board - Motherboard

- 2 XC2VP70 FPGAs
  - DUT configuration scrubber
  - DUT functionality monitor
- External interfaces
  - Platform flash devices
  - System ACE
  - Triple majority voted flash
  - 7 40-pin IDE connectors
  - 3 512-MB SDRAM DIMMs
  - 3 RS-232 ports
  - JTAG/Debug headers
  - MGT clock synthesizer
  - SMPX MGTs
IUCF Test Facility

- Indiana University Cyclotron Facility
  - Bloomington, IN
  - Proton beam
    - Energy: 30 - 200 MeV
    - Flux: $1 \times 10^2 - 1 \times 10^{11}$ p/sec-cm
  - Cable length distance to user area is 60-70 ft.

Test Setup

[Diagram showing the test setup with labeled connections and devices]
Test Setup Pictures

User Area

Petrick MAPLD05/BOFL146

Test Applications

1. Static Register/Cache Test
   - PowerPC initializes registers before each run
   - XMD used to initialize data cache before run, read out register and data cache after run via JTAG

2. “Pseudo-Static” Register Test
   - FuncMon issues IRQs to DUT PowerPC at 1-Hz
   - DUT PowerPC ISR dumps all 80 register values to FuncMon via 32-bit GPIO data bus
   - FuncMon buffers all data received, issues IRQ to its own PowerPC, which dumps data out UART
   - FuncMon also counts reset events and timeout events
Test Application Diagram

Test Complications

- Functionality not integrated for this test
  1. Configuration scrubbing
  2. Design triplication
  3. DUT PowerPC exception handlers
- Connection failures with socketed DUT card
  - 1152-pin spring loaded socket
  - Damaged springs resulted in signal connections including JTAG
  - Static register/cache test was not possible with socketed card
**SEE Results**

**Static Test Bit-Error Results**

<table>
<thead>
<tr>
<th>PowerPC Unit</th>
<th>Total Bit-Errors</th>
<th>Cross (cm²)</th>
<th>StDev</th>
<th>Cross/bit (cm²)</th>
<th>StDev</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPRs</td>
<td>4</td>
<td>4.99E-11</td>
<td>2.50E-11</td>
<td>4.88E-14</td>
<td>2.44E-14</td>
</tr>
<tr>
<td>D-Cache</td>
<td>87</td>
<td>4.34E-9</td>
<td>2.33E-10</td>
<td>3.31E-14</td>
<td>1.78E-15</td>
</tr>
</tbody>
</table>

**Pseudo-Static Test SEE Results**

(Note: Each run was stopped when the DUT stopped responding to IRQs)

<table>
<thead>
<tr>
<th>Computation Method</th>
<th>Cross (cm²)</th>
<th>StDev</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average of 24 runs</td>
<td>9.54E-10</td>
<td>7.51E-10</td>
</tr>
</tbody>
</table>

- Other observed effects:
  - Processor resets, DUT power cycling required, instruction jumps, program exceptions, irregular response to IRQs, bit-flips in SPRs

**Discussion of Results**

- **Static Test**
  - Valid SEU data collected on register and cache
  - For statistical purposes, more testing is required
  - Scrubbing will keep JTAG routing valid, decreasing the number of “bad” runs

- **Pseudo-Static Test**
  - The runs were not long enough to gather SEU data on the registers
  - Four runs failed during a DUT PowerPC ISR, *however*:
    - No scrubbing → all runs most likely failed due to configuration upsets rather than a PowerPC SEE
  - Scrubbing and exception handlers will allow SEU data to be collected using this IRQ design scheme
Future Work Plan

- Integrate configuration scrubbing, exception handlers, and TMR into designs
- Add more functionality to test applications
  - Use of dual PowerPCs for data collection
  - Ability to monitor/count program exception types
- Advanced test applications
  - Exercise PowerPC with dynamic test
  - Preliminary PowerPC mitigation test
- Next test date: October 17-19 @ IUCF