MICRON DDR2 SDRAM SEE TEST REPORT

Test Date: 11/11-11/15/07 **Report Date: 1/16/08**

I. Introduction

This reprot describes the SEE testing and characterization of the Micron MT47H128M8HQ-3:E 1G DDR2 SDRAM for NEPP (NASA Electronic Parts and Packaging Program). It is extends the testing done on other DDR2 SDRAMs with similar feature sizes from Samsung and Elpida during June and August of 2007 at the Texas A&M University Cyclotron Facility (TAMU) for parts from Samsung. Micron devices were irradiated with heavy ions to determine their sensitivity to SEU, MBU and SEFI and SEL. SEU and SEFI were seen even at the lowest test LET. SEL was seen at both room temperature and elevated at a temperature of 75 °C.

II. Device Description

The Micron 1G DDR2 SDRAMs are volatile memories that store data on a DRAM-type memory cell. Information can be written or read on both the rising and falling edges of the clock, effectively doubling device speed. Pin out is shown in figure 1. Detailed device information is provided in Table A-I.

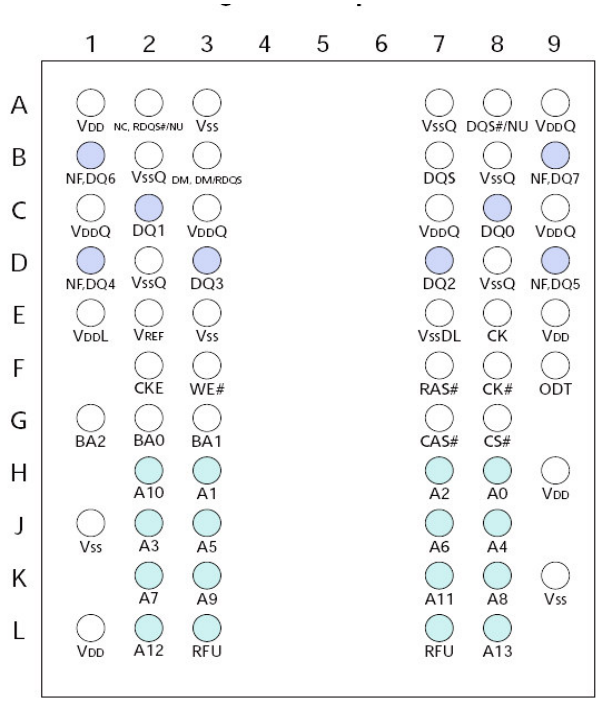


Figure 1 Pinout for the DDR2 package

III. Test Conditions

Test Temperature: Room Temperature
Operating Frequency: ≥400 MHz
Power Supply Voltage: biased at 1.8V.
Test Mode: Self-refresh [Melanie—please fill in additional details]

IV. Test Method

The testing was done at the Texas A&M University Cyclotron Facility (TAMU) with test parts thinned to roughly 150 microns. Irradiation was from the back side, using the 25 MeV/amu tune. Table I gives ions likely to be used in the test:

Table I: Test Ions at TAMU (25 MeV tune)

Ion	**LET ($MeV \cdot cm^2/mg$)**
Ne	1.7
Ar	5.4
Kr	19.3
Xe	37.9

The main goal of this test was to determine the susceptibility of the parts to SEL. A second goal was to map out the sensitivities of these devices to SEFI, MBU, SEU and stuck bits.

V. Device characterization

Testing was done with the GSFC High-Speed Digital Tester, which can write multiple test patterns including, all ones, all zeroes, checkerboard, and checkerboard complement. Parts have a nominal 2.5 V power supply, and an internal voltage of 1.8 V. During irradiation, power supply current was monitored for latchup. The test setup could be configured to run both with current limiting to protect parts from failure if possible and without to determine whether the SEL mode is destructive (or susceptible to latent damage) or not. As long as the sample was fully functional after latchup, we used it again for the next run.

Testing was done first at room temperature and then at 85 °C using the 24.8 MeV/amu beam tune at TAMU. Angles to the normal were chosen to achieve effective LET values other than the ones listed in Table I, and according to the ability of the ion to penetrate to the sensitive volume of the device. LET was estimated by transporting the ion through the overlayers of the device to the sensitive area.
Tests were run over all four test patterns—all 0's, all 1's, checkerboard and inverse checkerboard—to look for pattern dependence of SEU rates, as well as over ions and angles.

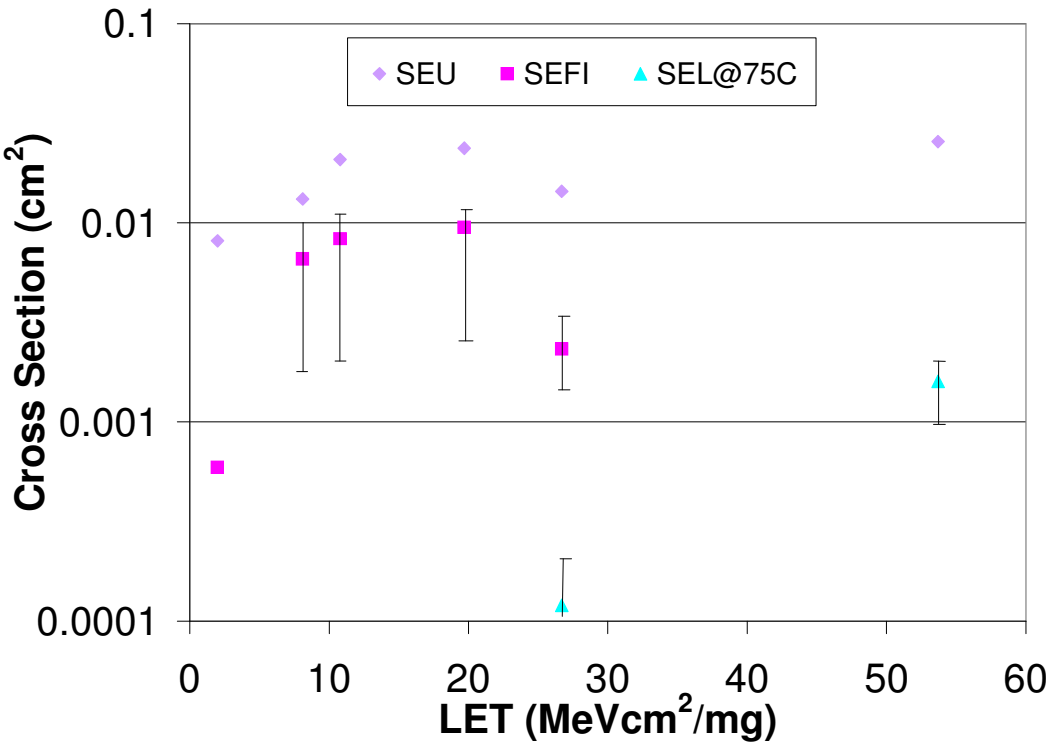
VI. Data Analysis

Because the Micron DDR2 SDRAM was susceptible to a both SEU and SEFI at low LET, the data analysis for this device was complicated. In many cases, SEFI cross sections were a substantial fraction of SEU cross sections, so SEU statistics were limited, especially at high LET, where SEFI sometimes occurred before the first SEU was recorded. (Note: since it takes about a minute to read the entire memory, the chances of this are not negligible.) SEUs were compared to the expected pattern to determine whether they involved multiple bit flips (in the same logical word). Any such upsets were

classified as multibit upsets (MBU). SEFI were identified by a burst of errors that occurred at or near the same time, or by recurrent errors affecting the same block, row or column. Stuck bits and SEL were identified in real time during testing—by recurring errors that persisted when the beam was off and by abrupt current increases, respectively.

VII. Test Results

The Micron DDR2 SDRAM proved to be susceptible to a variety of SEE modes, including SEU, SEFI, single-event stuck bits and SEL. SEL was seen at elevated temperature with an onset LET of about 26 MeVcm^2/mg, and at room temperature with an onset LET of about 33 MeVcm^2/mg. SEL currents were below maximum device specifications as well as trigger levels for SEL protection circuitry. In an attempt to distinguish between SEL and overcurrent due to bus contention, we issued a DUT reset once an overcurrent was seen. We found that this often resulted in a further current increase and triggered the SEL protection circuitry. Also, we noticed that if irradiation continued after an SEL was seen, the latchup current would increase in a stepwise fashion with time/fluence. Similar behavior was seen in the Hitachi/Elpida HM5225 family 256 Mbit SDRAMs. Laser testing of this device revealed that this behavior resulted from sequential activation of multiple independent SEL susceptible nodes in the device's control logic.



Because of the difficulty of assessing the health of the device once a SEFI had occurred, we did not attempt to distinguish between SEFI and block errors. From the error output, it appears that the vast majority of SEFIs resulted in a near complete loss of device functionality.

Generic Part Number:	
Full Part Number	MT47H128M8HQ-3:E
Manufacturer:	Micron
Lot Date Code (LDC):	
Quantity Tested:	3
Serial Numbers of Control Sample:	1
Serial Numbers of Radiation Samples:	2, 3, 4, 5, 6
Part Function:	DDR2 SDRAM
Part Technology:	90 nm CMOS
Case Markings:	Micron MT47H128M8HQ-3:E
Package Style:	68 pin FBGA, thinned
Test Equipment:	Power Supply (+2.5V) Digital test board. Multimeters
Test Engineer:	M. Berg, H. Kim
Dose Levels (krad (Si)):	N/A
Target dose rate (rad (Si)/min):	N/A

VIII. **Table I**. Device information

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
F3, B3	B3	LDM, UDM DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
K9	F9	ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
K7, L7, K3	F7, G7, F3	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ2, DQ3–DQ5, DQ6–DQ8, DQ9–DQ11, DQ12–DQ14, DQ15	I/O	**Data input/output:** Bidirectional data bus for 64 Meg x 16.
–	C8, C2, D7, D3, D1, D9, B1, B9	DQ0–DQ2, DQ3–DQ5, DQ6–DQ7	I/O	**Data input/output:** Bidirectional data bus for 128 Meg x 8.
–	C8, C2, D7, D3	DQ0–DQ2, DQ3	I/O	**Data input/output:** Bidirectional data bus for 256 Meg x 4.
–	B7, A8	DQS, DQS#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7, E8	–	LDQS, LDQS#	I/O	**Data strobe for lower byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
B7, A8	–	UDQS, UDQS#	I/O	**Data strobe for upper byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B3, A2	RDQS, RDQS#	Output	**Redundant data strobe:** For 128 Meg x 8 only. RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
A1, E1, M9, R1, J9	A1, E9, L1, H9	V_{DD}	Supply	**Power supply:** 1.8V ±0.1V.

x16 Ball Number	x4, x8 Ball Number	Symbol	Type	Description
A9, C1, C3, C7, C9, G3, E9, G1, G7, G9,	A9, C1, C3, C7, C9	VDDQ	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
J1	E1	VDDL	Supply	**DLL power supply:** 1.8V ±0.1V.
J2	E2	VREF	Supply	SSTL_18 reference voltage (VDDQ/2).
A3, E3, J3, N1, P9	A3, E3, J1, K9	VSS	Supply	Ground.
J7	E7	VSSDL	Supply	**DLL ground**: Isolated on the device from VSS and VSSQ.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8	A7, B2, B8, D2, D8	VSSQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
A2, E2	–	NC	–	**No connect:** These balls should be left unconnected.
–	B1, B9, D1, D9	NF	–	**No function:** x8: these balls are used as DQ4–DQ7; x4: they are no function.
A8, E8	–	NU	–	**Not used:** For x16 only. If EMR(E10) = 0, A8 and E8 are UDQS# and LDQS#. If EMR(E10) = 1, then A8 and E8 are not used.
–	A2, A8	NU	–	**Not used:** For x8 only. If EMR(E10) = 0, A2 and E8 are RDQS# and DQS#. If EMR(E10) = 1, then A2 and E8 are not used.
R8, R3, R7	L3, L7	RFU	–	**Reserved for future use:** Row address bits A13 (x16 only), A14, and A15.