1. INTRODUCTION

This study is being undertaken to determine the single event destructive and transient susceptibility of the RTAXS Family FPGAs. The devices will be monitored for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing them to a heavy ion beam at the Texas A&M University Cyclotron Single Event Effects Test Facility. The objective of the study is to determine Bit Error Rates (BER) per day within a synchronous design implemented within a commercial SRAM based FPGA device and the BER’s dependency on: Clock Frequency, Design Architecture (amount of combinatorial logic vs. Sequential logic), and Data pattern (Data Frequency).

2. DEVICES TESTED

There were 6 different architectures tested 2 parts each. The sample size per device (in this case) was not the focus since they are production- high speed parts with very little variation across the CMOS process. The emphasis was to test variations over the design state space. The devices were manufactured on an advanced 0.15um CMSOS Antifuse Process Technology with 7 layers of metal. The manufacturer is Actel. The devices tested had Lot Date Codes of 0506 and 0543.

Purpose is to investigate SEU Frequency Data Pattern, and Architectural Dependencies. SEU testing targets speeds from 18.75MHZ up to 150 MHZ.

2.1 DUT Architecture

The Principle Configuration is a shift register string (700 to 8000 DFF’s) with varying levels of combinatorial logic (0, 4 or 8 inverters between DFF’s) and Fanout options to the Enable inputs. A By-4 clock divider circuit is implemented to shift the last 4 bits of the Shift register string into a DFF window (SCAN_DATA). The window is output to the tester. A data clock (SHIFT_CLK) is also output to the tester for high speed synchronous data capture. Reset passes through an asynchronous assert – synchronous de-assert circuit and is supplied to every DFF.
The following is the reset circuit used within the DUT.

The following is the DUT configuration schematic:

---

**Figure 1: Asynchronous Assert - Synchronous De-assert**

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The following is the DUT configuration schematic:
DUT Top Level Architecture

Figure 2: Device Under Test Top Level Architecture
The following demonstrates details of the shift register strings.

\[ N = 0, 4, \text{or} 8 \text{ inverters} \]

Figure 3: Shift Register String with Optional Combinatorial Logic

Various levels of combinatorial logic are used in order to measure possible transient susceptibility. If the RTAXS device is susceptible to transients, then faults will be frequency dependent. Fan-out to the enables is used to investigate multiple bit hits and the hardness of the enable MUX that is within every RTAXS DFF primitive. A string length of 700 and 800 are tested with and without the combinatorial logic. A string length of 8000 is tested without the combinatorial logic in order to insure that the additional faults are not from the larger area of the additional combinatorial logic.
3. TEST FACILITY

3.1 Heavy Ion.

**Facility:** Texas A&M University Cyclotron Single Event Effects Test Facility, 15 MeV/amu tune.

**Flux:** 1.0E04 to 2.0E05 particles/cm²/s

**Fluence:** All tests were run to 1 x 10⁷ p/cm² or until destructive or functional events occurred.

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MEV/Nucleon)</th>
<th>LET (MEV/cm²/mg) 0 deg</th>
<th>LET (MEV/cm²/mg) 45 deg</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ar</td>
<td>15</td>
<td>8.5</td>
<td>12</td>
</tr>
<tr>
<td>Cu</td>
<td>15</td>
<td>20.7</td>
<td></td>
</tr>
<tr>
<td>Kr</td>
<td>15</td>
<td>28.5</td>
<td>40.26</td>
</tr>
<tr>
<td>Xe</td>
<td>15</td>
<td>52.7</td>
<td>74.5</td>
</tr>
</tbody>
</table>

3.2 Proton

Tests were performed at two facilities.

**Facility:** Crocker Nuclear Laboratory (CNL) at the University of California at Davis (UCD)

**Flux:** 1.0E09 particles/cm²/s

**Fluence:** All tests were run to 7.14E11 p/cm²

**Energy:** 63 Mev-protons

**Facility:** Indiana University Cyclotron Facility (IUCF)

**Flux:** 3.0E9 particles/cm²/s

**Fluence:** All tests were run to 1.0E12 p/cm²

**Energy:** 195 MeV - incident
4. TEST CONDITIONS

Test Temperature: Room Temperature
Operating Frequency: 15 MHZ to 150MHZ
Power Supply Voltage: 3.3v I/O and 1.5V Core.

5. TEST METHODS

5.1 Architectural Overview

The RTAX-S controller/processor is instantiated as a sub component within the Low Cost Digital Tester (LCDT). The LCDT consists of a Mother Board (FPGA Based Controller/Processor) and a daughter board (containing DUT and its associated necessary circuitry). The socket within the DUT Daughter board can accommodate the RTAX1000S and RTAX2000S devices. The objective of this DUT Controller/processor is to supply inputs to the RTAX-S ACTEL Device and perform data processing on the outputs of the RTAX-S. The LCDT communicates with a user controlled PC. The user interface is LAB-VIEW. It will send user specified commands to the mother board and receive information from the mother board. Please see Documents: “LCDT” and “General Tester” for further information concerning the LCDT functionality. The LCDT is connected to the RTAX DUT as shown in the following Block Diagram.
Figure 4: System Level Tester Architecture

5.1.1 I/O List and Definitions

Table 2: I/O Table

<table>
<thead>
<tr>
<th>Input Name</th>
<th>Description</th>
<th>Direction</th>
<th>Synchronous</th>
<th>Slew</th>
<th>Pullup</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>System clock of the LCDT</td>
<td>Input</td>
<td>Clock</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>RESET</td>
<td>LCDT system reset</td>
<td>Input</td>
<td>A</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>RX232</td>
<td>Serial receive input</td>
<td>Input</td>
<td>A</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>SCAN_DATA(4:0)</td>
<td>Data window of RTAX-S. Data is processed by LCDT and compared against</td>
<td>Input</td>
<td>A</td>
<td>N</td>
<td></td>
</tr>
</tbody>
</table>
### 5.2 Requirements

The requirements for the RTAX-S LCDT tester are listed in Table 3.

<table>
<thead>
<tr>
<th>Item</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Supply System Clock to the RTAX-S</td>
</tr>
<tr>
<td>2</td>
<td>Supply Reset to RTAX-S</td>
</tr>
<tr>
<td>3</td>
<td>Supply Data Input to the RTAX-S</td>
</tr>
<tr>
<td>4</td>
<td>Clock Frequency of RTAX-S shall be variable</td>
</tr>
<tr>
<td>5</td>
<td>Maximum RTAX-S input clock frequency shall be 150Mhz</td>
</tr>
</tbody>
</table>
0, 1, and checker board data patterns shall be generated and placed on the RTAX-S data lines

RTAX-S reset shall be active low

RTAX-S reset shall be active for at least 3 RTAX-S system clocks

RTAX-S Data Inputs shall be stable at the Rising Edge of the RTAX-S system clock with a set-up time of 3ns and a hold time of 3ns

RTAX-S data inputs shall be captured by the LCDT data processing module once detecting the rising edge of the data clock (SHIFT_CLK)

SHIFT_CLK rising edge detection must include a metastability filter because the SHIFT_CLK input is asynchronous.

Input Data must be registered before the data processing block implements the compares – protects against radiation induced I/O transients.

Data processing block shall report every error to the FIFO block

The tester supplies inputs as follows: Data (D_SR) changes at the falling edge of the input clock (CLK_SR) so that it is stable and can be captured at the rising edge. CLK_SR and D_SR will be at the user specified frequency. The user will also supply the actual data pattern. Data patterns range from all 0’s, all 1’s, and alternating 1’s and 0’s.

<table>
<thead>
<tr>
<th>6</th>
<th>0,1, and checker board data patterns shall be generated and placed on the RTAX-S data lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>RTAX-S reset shall be active low</td>
</tr>
<tr>
<td>8</td>
<td>RTAX-S reset shall be active for at least 3 RTAX-S system clocks</td>
</tr>
<tr>
<td>9</td>
<td>RTAX-S Data Inputs shall be stable at the Rising Edge of the RTAX-S system clock with a set-up time of 3ns and a hold time of 3ns</td>
</tr>
<tr>
<td>10</td>
<td>RTAX-S data inputs shall be captured by the LCDT data processing module once detecting the rising edge of the data clock (SHIFT_CLK)</td>
</tr>
<tr>
<td>11</td>
<td>SHIFT_CLK rising edge detection must include a metastability filter because the SHIFT_CLK input is asynchronous.</td>
</tr>
<tr>
<td>12</td>
<td>Input Data must be registered before the data processing block implements the compares – protects against radiation induced I/O transients.</td>
</tr>
<tr>
<td>13</td>
<td>Data processing block shall report every error to the FIFO block</td>
</tr>
</tbody>
</table>

Clock

<table>
<thead>
<tr>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<tr>
<td></td>
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</tbody>
</table>

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5.3 User Interface and Control

The User controls the tests via a LABVIEW interface running on a PC. The PC communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word.

<table>
<thead>
<tr>
<th>Command #</th>
<th>Command</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Reset DUT</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>Resets RTAX-S</td>
</tr>
<tr>
<td>02</td>
<td>Start Test</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>Starts RTAX-S clock and data generation</td>
</tr>
<tr>
<td>90</td>
<td>Pattern Number</td>
<td>Y</td>
<td>N</td>
<td>N</td>
<td>0,1,or checker board</td>
</tr>
<tr>
<td>A0</td>
<td>Clock Frequency</td>
<td>Y</td>
<td>N</td>
<td>N</td>
<td>Clock frequency divider of 150mhz</td>
</tr>
</tbody>
</table>

The following is a detailed description of commands and their associated functionality.

5.3.1 **RESET DUT:**

The RESET DUT command is decoded as x01. The following represents the command as noted in Table 4:

![Figure 5: Reset Command Format – Command Number, D0, D1, and D2](image)

Once decoded, all DUT inputs will go into reset mode (Reset, CLK_SR and D_SR are low).

5.3.2 **START TEST:**

START TEST is decoded as x02. The following represents the command as noted in Table 4:

![Figure 6: Start Command Format](image)

All other commands should be supplied before start test. I.e. the user should define the pattern and clock frequency before administering a start. This command activates the CLK_SR and D_SR DUT inputs.
5.3.3 PATTERN NUMBER:

There are three data patterns that can be generated by the tester. Data can be a static 0, a static 1, or alternate every RTAX-S clock cycle (checker board). The command number is x90. The first byte of data (D0) is also decoded (all other bytes are ignored but must be supplied – i.e. all commands must be 4 bytes of data).

\[
\begin{array}{cccc}
\text{x90} & \text{x00} & \text{xx} & \text{xx} \\
\text{x90} & \text{x01} & \text{xx} & \text{xx} \\
\text{x90} & \text{x02} & \text{xx} & \text{xx} \\
\end{array}
\]

Figure 7: Pattern Command Format

D0 decode is as follows:
X00: Static 0
X01: Static 1
X02: Checkerboard Pattern

5.3.4 CLOCK FREQUENCY:

The clock frequency command is decoded as xA0 and D0. The following represents the command as noted in Figure 8:

\[
\begin{array}{cccc}
\text{xA0} & \text{xx} & \text{xx} & \text{xx} \\
\end{array}
\]

Figure 8: Clock Frequency Command Format

Upon the receipt of this command, D0 is used as a clock frequency divider. This command must be sent after a RESET DUT and before a START TEST. D0 must be an even number and must be greater than or equal to 2. The associated output is CLOCK_FREQ. See the LCDT General Tester for more information concerning the processing of CLOCK_FREQ.

5.4 Processing the DUT Outputs

The outputs of the DUT are fed to the tester for data processing. The objective of the data processing is to synchronously capture data using SHIFT_CLK (as a data enable) and SCAN_DATA (as a 4 bit window of DUT Data). SHIFT_CLK has a maximum frequency of 37.5MHZ (150 MHZ divided by 4). It is a control signal indicating new data. It is considered asynchronous to the tester and is sampled using the tester’s system clock (max 150 MHZ). Thus, the tester’s sampling clock will always be 4 times as fast
as SHIFT_CLK. The SHIFT_CLK is fed into a metastability filter and an edge detect. This process takes 1 to 2 clock cycles of the sampling clock (detection will be delayed by 1 to 2 sampling clock cycles of the actual edge). Once the edge is detected, data is then sampled and registered. The data is then registered again. The comparison is made against the second registered data and if there is a mismatch, the error is reported.

Figure 9: Timing Diagram of Expected DUT Outputs

6. HEAVY ION RESULTS: TEXAS A&M UNIVERSITY

The RTAXS devices were irradiated with Argon, Copper, Krypton, and Xenon beams at normal incidence, 0 and 45 degrees (yielding effective LETs of approximately 8.5, 12, 28.5, 40.26, 52.7, 74.5 MeV•cm²/mg) at the Texas A&M University Cyclotron Single Event Effects Test Facility (please refer to Section 3 Test Facility). Faults from the RTAXS devices were encountered at all LETs at 150MHZ. However, the number of SEUs was very low at Argon.

The RTAXS devices were tested to measure the Single Event latchup cross section under the above conditions. Each part was placed in the beam until a Single Event latch (SEL) event occurred or 10⁷ ions/cm² – the beam fluence was then recorded. During our experiment, no Single Event latchup events occurred, yielding a threshold SEL LET for latchup of > 74.5 MeV•cm²/mg.

The RTAXS devices were also tested to measure the error cross section under the above conditions. Each part was placed in the beam until 10⁷ ions/cm² was reached. An
average cross section per bit was determined for a given LET as the number of fault events observed divided by the total fluence of the associated run at that LET.

6.1 Preliminary Results
Results from the initial test trip demonstrated a significant difference in error cross-section over frequency and DUT architecture. Due to the increased frequency response with DUTs containing more combinatorial logic, it is clear that transients have an affect on the implemented design.

Figure 10: LET vs. Error Cross Section: Preliminary Data Demonstrating Frequency Response Variation across Architectures.
Non-traditional SEU effects were observed: Current increases noted with number of particles used for irradiation in every test run. Upon power cycling the device, residual current disappeared (i.e. it was not a hard fault). Occurrence was consistent with Actel data sets. The problem has been fixed with a newer version of Actel’s programmer. See Actel’s presentation in this Briefing for detailed discussion of data, root cause (back end software), and fix.
6.2 Cross Section with respect to LET

As the LET value increases, so does the transient width. Results demonstrate that the number of faults due to transient capture also increases. Architectures with different levels of combinatorial logic were tested at various frequencies. 4F4L (4 extra levels of combinatorial logic) is compared to 0F0L (no extra levels of combinatorial logic) At higher LET values the separation between cross section are evident.

Figure 12: Comparison of two Architectures: Cross Section and LET @ 150MHZ – Data Pattern = Alternating
6.3 Bit Error Rate Calculations

Using the CREME96 at worst case GEO, the errors-bit/day were:

- 15MHZ and no extra level of combinatorial logic (0F0L) : < 5E-9
- 150MHZ and 4 levels of extra combinatorial logic (4F4L) : <5E-8

The results show a very large difference compared to the ACTEL reported data sheet value of <4E-11.

6.4 Architectural and Frequency Effects

At each LET, several tests were performed at various frequencies on all of the shift register string types. As the frequency increased, the cross-section increased. The relationship is linear through out all shift register strings. Based on theory (see Figure 13), a shift register string of hardened (TMR) DFFs should not see a significant increase in its error cross-section over frequency because DFF SEUs are not frequency dependent. However, the DFF primitive within the RTAXS series contains additional combinatorial logic. This is where the frequency effects originate.
The shift register strings containing combinatorial logic (4F4L, 0F4L, 8F8L) have a significantly larger error cross section per bit than the shift register strings that do not
contain additional combinatorial logic (0F0L). This suggests that the DFFs are hardened (as expected) and are safer circuitry to implement within a design, than the combinatorial logic. However, it is important to note that there were faults observed with the 0F0L architecture. This is due to the extra logic (not illustrated in Figure 14) that is contained in an instantiated RTAX-S RCELL.

Figure 15: LET = 74.5 MeV*cm²/mg, data pattern = checkerboard

There exist approximately two orders of magnitude of difference between the 15 MHZ-0F0L point and the 150MHZ-4F4L point.
6.5 Data Pattern Effects

In order to investigate data pattern effects, multiple architectures were analyzed at several LET values, frequencies with each data pattern (static zero, static one, and alternating ones and zeros). The 700 8F8L and 4F4L string (implemented within the RTAX1000) were compared – data points were statistically equal (see Figure 15). The Normalized cross sections of the 800 count 0F0L string (implemented within the RTAX 2000) and the 8000 count 0F0L string were compared. Their cross sections were also statistically equal.

Static data input yielded lower error cross sections than the alternating data pattern for all shift register strings. While comparing extreme cases (0F0L static 0-pattern to a 700 4F4L alt-pattern) there is over a magnitude of difference in the error cross section. It is important to note that the results of the testing demonstrate the importance of data pattern and architectural choice.
Figure 17: 4F4L Data Patterns at 18.8 MHz and 150 MHz
6.6 Bursts

Because of the synchronous nature of the tester in respect to the DUT, it is possible to capture, and analyze data every clock cycle (even at its highest speed – 150MHZ). Every fault is time stamped and a burst counter is incremented if there is a fault in the following clock cycle (as just previously analyzed – novel approach). This methodology of testing affords the analysis an increase in visibility to fault data interpretation.

Bursts were seen only at LET values greater than 53 Mev*cm²/mg. When bursts were values of long strings of “0” with the existence of a SHFT_CLK no matter the data pattern – bursts were assumed to be on the reset line. There were some occurrences when there was a loss of the (SHFT_CLK) with no recovery (only upon system reset)– the source has not been determined. However, recoverable (or temporary) SHFT_CLK+data loss is considered to be a clock upset.

7. PROTON RESULTS
The following is a summary of the results from the separate proton test trips/facilities (please refer to Section 3 Test Facility)
7.1 Proton dose levels (63 MeV protons) of 100 to 200 krads(Si) per device.

No SEUs observed at 15 MHz for any string. Few SEUs observed at worst case 150 MHz. SEU Cross-section of 6.65E-16 cm$^2$ per device for 4F4L. There is roughly an order of magnitude confidence level on results (low statistics). There were no SEUs observed on other DUT strings at 150 MHz.

7.2 Proton dose levels (195 MeV protons) of 300 krads(Si) per device

There were no SEUs observed at 18.75 MHz for any string. Just a few SEUs observed at worst case 150 MHz. A SEU Cross-section of 8.5E-16 cm$^2$ was calculated per device for 0F0L and a SEU Cross-section of 2.8E-16 cm$^2$ was calculated per device for 4F4L.

8. RECOMMENDATIONS

In general, devices are categorized based on heavy ion test data into one of the four following categories:

- Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
- Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
- Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
- Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications.

Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications.

The RTAXS series FPGAs are Category 2 devices.

9. FURTHER TEST REQUIREMENTS

It is suggested that the RTAXS series memory be tested by the NASA GODDARD Radiation and Effects Group. Data patterns, frequencies, and scrubbing rates will be investigated.

9.1 Appendix 1: