Effects of Heavy Ion Exposure on Nanocrystal Nonvolatile Memory

Timothy R. Oldham
Radiation Effects and Analysis Group
QSS Inc
Seabrook, MD, 20706 USA
Timothy.Oldham@gsfc.nasa.gov

Hak Kim
Aerospace Engineering Division
Jackson and Tull Chartered Engineers
Greenbelt, MD 20771 USA

Mohammed Suhail, Peter Kuhn, and Erwin Prinz
Technology Solutions Organization
Freescale Semiconductor
Austin, TX-78735 USA

Kenneth A. LaBel
Goddard Space Flight Center
Radiation Effects and Analysis Group, Code 561.4
Greenbelt, MD 20771

***Abstract*—Advanced nanocrystal nonvolatile memories have been exposed to heavy ion bombardment. They appear to be promising candidates for future spacecraft electronics.**

Keywords-component; electronics, nonvolatile memory, anaocrystals, radiation effects

I. INTRODUCTION

We have irradiated engineering samples of Freescale 4M nonvolatile memories with heavy ions. They use Silicon nanocrystals as the storage element, rather than the more common floating gate. The irradiations were performed using the Texas A&M University cyclotron Single Event Effects Test Facility. The chips were tested in the static mode, and in the dynamic read mode, dynamic write (program) mode, and dynamic erase mode. All the errors observed appeared to be due to single, isolated bits, even in the program and erase modes. These errors appeared to be related to the micro-dose mechanism. All the errors corresponded to the loss of electrons from a programmed cell. The underlying physical mechanisms will be discussed later. There were no errors, which could be attributed to malfunctions of the control circuits. At the highest LET used in the test (85 MeV/mg/cm^2), however, there appeared to be a failure due to gate rupture. Failure analysis is being conducted to confirm this conclusion. There was no unambiguous evidence of latchup under any test conditions. Generally, the results on the nanocrystal technology compare favorably with results on currently available commercial floating gate technology, indicating that the technology is promising for future space applications, both civilian and military.

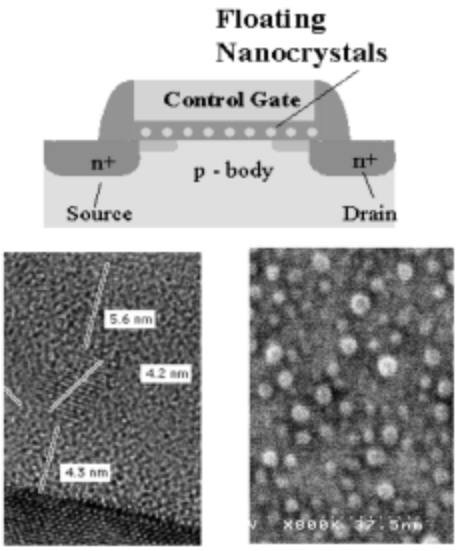

Figure 3. Silicon nanocrystal nonvolatile memory bitcell showing the floating silicon nanocrystals used for isolated charge storage.

II. DESCRIPTION OF DEVICES

The test chips were experimental 4Mb Flash EEPROM memories fabricated using 0.13µm design rules. Nanocrystal technology is a new approach for non-volatile memory that may eventually replace the established floating gate technology. In this technology the storage medium consists of a layer of silicon nanocrystals, sandwiched between a bottom and a top oxide, instead of the continuous polysilicon storage medium of floating gate technology. The use of silicon nanocrystals (Figure. 1) as a storage medium has shown to provide immunity from oxide defects which can arise during program / erase operations and to enable reduction of dielectric thicknesses and therefore lower operating voltages. The nanocrystal technology has been described in more detail, elsewhere [1].

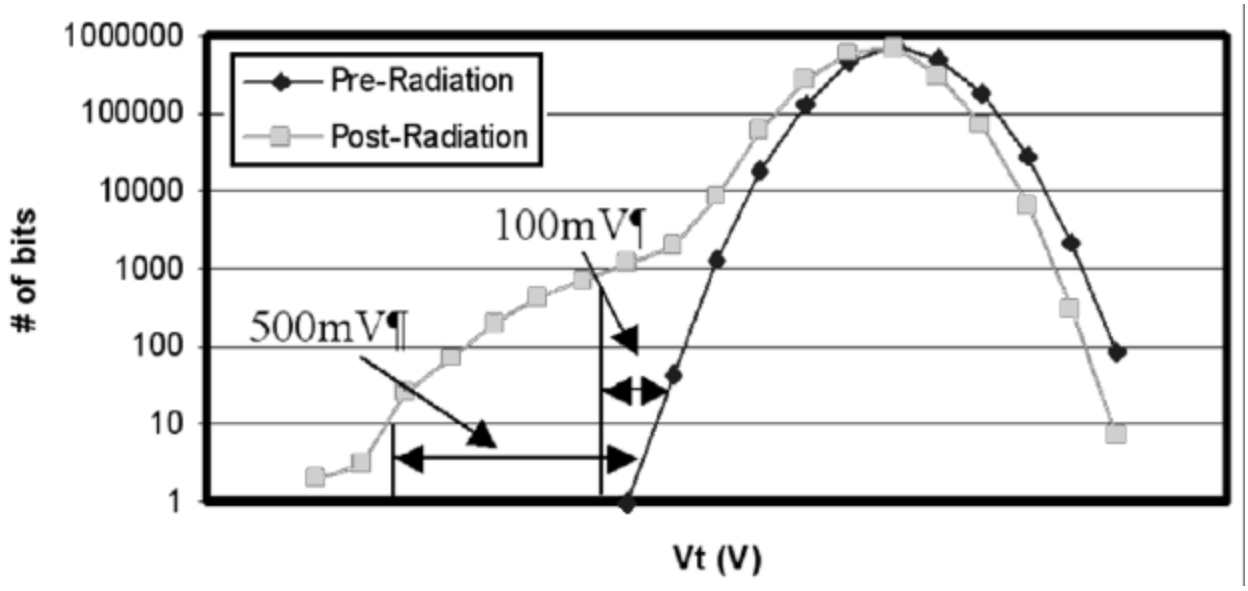

Figure 2. Program state threshold voltage distributions pre and post radiations.

III. TEST PROCEDURE

The testing was done using the SEETF (Single Event Effects Test Facility) at the Texas A&M Cyclotron, which was tuned to 15 MeV/nucleon, using the ions indicated in Table I. Each exposure was to a total fluence of 10^7 particles/cm^2.

TABLE I. ION TABLE

Ion	E(MeV)	LET (MeV/mg/cm^2)	Range (? m)
Ar	497	8.7	175
Kr	916	29.3	117
Xe	1299	53.8	102
Au	2247	85	118

The parts were tested in the static mode, in dynamic read mode, and dynamic program and erase modes. In the static testing, a pattern was written, and errors counted after the exposure. In dynamic read testing, a stored pattern was read continuously during the exposure, and the errors counted. The write or program mode was tested by continuously doing a write/read cycle. The erase mode was tested by cycling continuously through erase/write/read steps, and counting errors when the pattern read differed from the pattern expected. Patterns that could be written were all zeroes, all ones, checkerboard, and inverse checkerboard. Most of the testing was actually done with zeroes written, since that was the state sensitive to radiation.

IV. RESULTS

The errors appear to be all static bit flips, which are counted again each time the memory is read, in a dynamic test. That is, there appear to be no errors due to transients in the peripheral circuits, even during the high voltage write and erase steps. All the testing was done at relatively low frequency, so the failure to capture any SETs may not be surprising. But previous tests of floating gate memories had shown functional interrupts (SEFI) during program and erase tests [2-5].

All the static bit flips are zeroes turned into ones. When the cell is written into the zero state, electrons are injected into either the floating gate or the Silicon nanocrystal layer. The usual effect of ionizing radiation in a MOS structure is to introduce positive trapped charge in the oxide, which reduces the net effective negative stored charge, either by compensation or by recombination. For this reason, the threshold voltage (V_T) is reduced for transistors hit by an ion. If the threshold voltage is reduced below some critical value, the bit is read as a one (gate empty of electrons) rather than as a zero (gate full of electrons).

Figure. 2 shows the tail in the threshold voltage distributions post radiation. Similar behavior has been reported on floating gate bit-cells. [6-8]. The test vehicle used for this experiment has special test modes, which can be used to set the fail criteria. To maximize sensitivity without introducing noise into the measurement the fail criteria during this experiment was set to 100mV from the initial threshold distribution as shown in Figure 2. A product would have a much wider fail margin, typically >500mV. Figure 2 shows that the SEU would decrease by a two orders of magnitude if the fail criteria were set at a realistic target of 500mV.

For the nanocrystal technology, the results for stored zeroes are summarized in Figure 3. For the read tests illustrated in Figure. 3, the maximum bit error count was slightly more than 10^4, for 10^7 particles/cm^2. However, the area of the memory array is much less than a square cm, approximately 0.02 cm^2. Therefore, the number of ions hitting the array is on the order of $2x10^5$ per exposure. Perhaps 30 percent of the array area is active gate area (estimated from a SEM picture), so the number

of ions hitting active gate regions is about $6x10^4$ per exposure. In other words, about one ion out of 6 that hits the active gate area changes the state of the cell, even at the highest LET tested so far. Therefore, the observed cross section is about one sixth times the geometric gate cross-section.

The results of the dynamic write/read testing are summarized in Figure. 4. The errors appear to all be static single bit errors, and the total count is less than in the read only test, because the flipped bits are being rewritten during the test, instead of being allowed to build up. No functional interrupts were observed, nor any other errors that could be attributed to the control circuits.

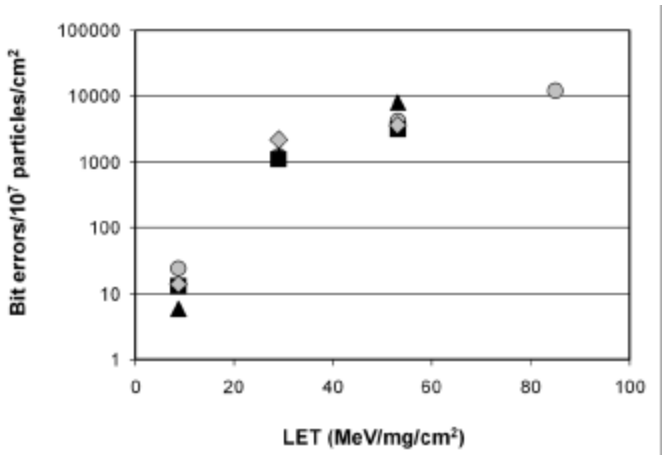

Figure 3. Read errors.

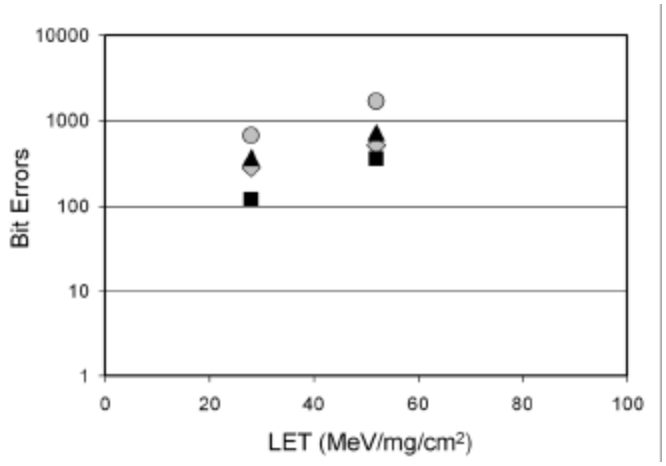

Figure 4. Dynamic read/write errors.

The results of the dynamic erase/write/read test are summarized in Figure. 5. Again, the errors appear to be all static single bit errors, where the total count is less than in the read only test, because the errors are being rewritten during the test. No functional interrupts were observed, nor any other errors that could be attributed to the control circuits.

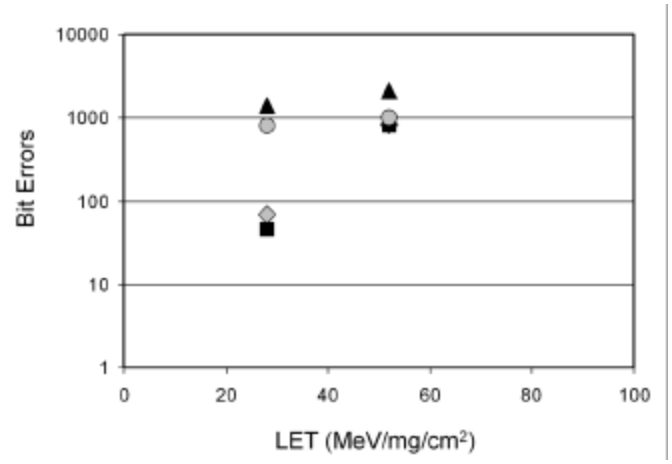

Figure 5. Dynamic read/write/erase errors.

No unambiguous latchup was observed at any time, but the circuit went into a high current state after most exposures at all LETs tested. The circuit was fully functional, even in the high current state, which suggests that it was not the result of a general latchup. It is possible that there was a micro-latch somewhere on the chip, however. In addition, there was a possible gate rupture in a read test with Au ions incident. There was a high current condition immediately after the exposure, which was eliminated by cycling the power to the chip. But the high current condition was restored by trying to exercise the chip, which suggests a short, somewhere. Failure analysis is being performed to determine the exact cause of this result.

V. DISCUSSION

The underlying mechanism for the bit errors appears to be related to the micro-dose—an ion deposits a small, dense cluster of positive charge, which neutralizes enough of the stored electrons on the storage element to change the state of the cell, either through recombination or compensation. This mechanism has been described most completely for normal gate oxides [9,10]. However, Cellere et al. [7] reported that the negative charge lost off floating gate devices irradiated with heavy ions was far greater than the amount of positive charge deposited by an ion. For this reason, the underlying mechanisms are not completely clear, and should be the subject of further study.

Figure. 2 shows the tail in the threshold voltage distributions immediately after radiation. The shift is caused by radiation induced charge loss from the silicon nanocrystals. The instantaneous shift in the threshold distributions can cause read errors, but no permanent damage is done to the bit-cell, and the data can be restored by resetting the array. In addition to the read errors, long term data retention performance of the radiated bit-cells after reset is of concern. It has been reported that the long-term data retention of the conventional floating gate bit-cells are impacted by radiation. [7, 8] A few possible theories have been proposed for the degradation in data retention performance of radiated bit-cells. [7, 8] It is generally accepted that changes to the oxide properties, leading to localized leakage paths, are the cause for long term data retention performance degradation of the floating gate bit-cells.

A localized leakage path due to oxide damage cannot cause data retention failure in a nanocrystal bit-cell as the charges are stored in discrete silicon nanocrystals. The long-term data retention of the nanocrystal memory is expected to be better than that of a floating gate bit-cell.

VI. CONCLUSION

The basic nanocrystal technology looks promising for space applications, since many of the effects observed in other nonvolatile memory technologies have not been observed. All the errors so far appear to be micro-dose effects in single cells, and the sensitivity is determined by the voltage margins, rather than any intrinsic characteristic of the underlying technology.

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