SEE Test Report
Cypress EZ-USB FX2 USB Microcontroller and
SMSC USB2512 USB Hub

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1. INTRODUCTION

The goal of this study is to determine the single event destructive and transient susceptibility of the Cypress EZ-USB FX2 USB Microcontroller device and the SMSC USB2512 USB Hub. The proposed test scheme involves detailed monitoring of DUT responses to heavy-ion beam exposure at Texas AM Cyclotron facility. The elaborate test setup has the capability of differentiating upset events within USB protocol packet sequencing and actual data errors via a customized USB tap circuit.

2. BACKGROUND

2.1 EZ-USB FX2 Microcontroller

The EZ-USB FX2 is a Single-Chip integrated USB 2.0 Transceiver, SIE, and Enhanced 8051 Microprocessor. It is a commercial grade IC with a variety of logic types including mixed-signal and CMOS circuits. Due to the complexity of the device, the heavy ion testing is not expected to pin-point circuit susceptibility. Instead, device susceptibility and Single Event Effects (SEE) error signatures will be characterized.

The architecture of the EZ-USB FX2 (see Figure 1) results in data transfer rates of 56Mbytes per second, the maximum allowable USB2.0 bandwidth. The EZ-USB FX2 operates at two of the three rates defined in the Universal Serial Bus Specification Revision 2.0:

- Full speed, with a signaling rate of 12Mbps
- High speed with a signaling rate of 480Mbps
- EZ-USB FX2 does not support the low-speed signaling mode of 1.5Mbps

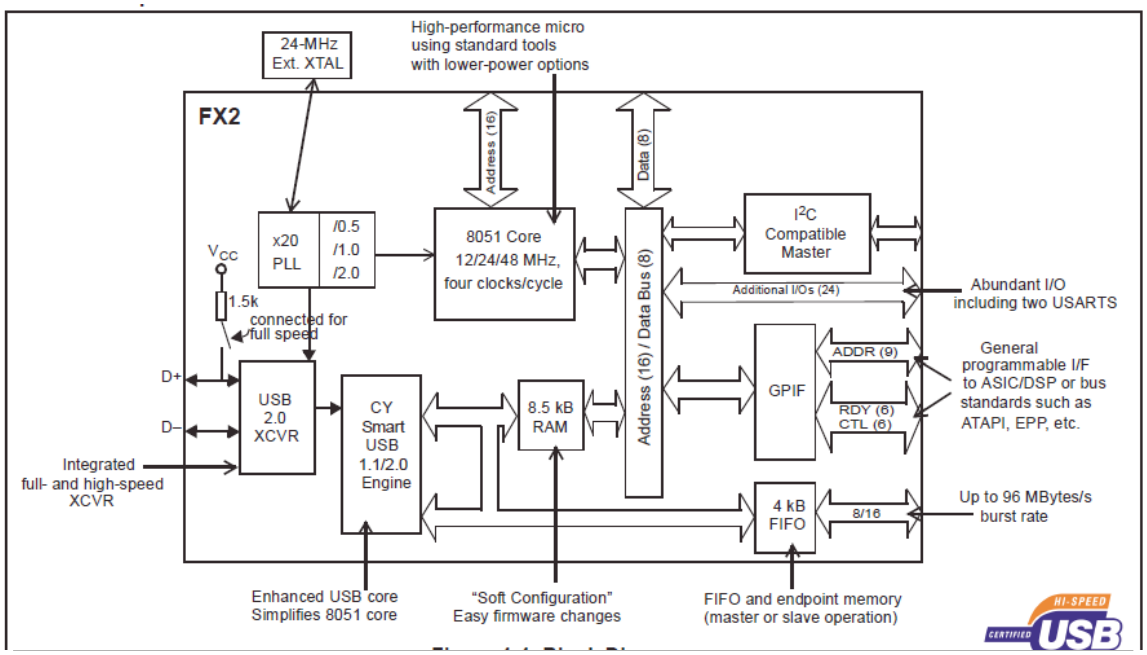

Figure 1: EZ-USB FX2 architecture

2.2 SMSC USB2512 USB Hub

The SMSC 2-Port Hub is a low power, OEM configurable, single transaction translator (STT) hub controller IC with 2 downstream ports for embedded USB solutions. The 2-port hub is fully compliant with USB 2.0 Specification. Figure 1 shows the block diagram of the device.

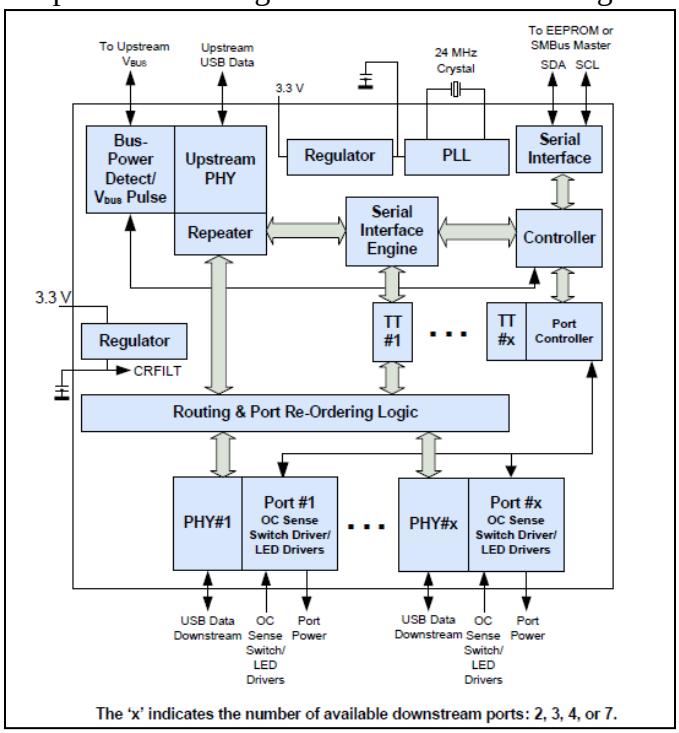

Figure 2. SMSC USB2512 block diagram.

2.3 Devices Tested

Both the EZ-USB FX2 Microcontroller and SMSC USB Hub are commercial devices and no lot data code is available.

3. LOW COST DIGITAL TESTER (LCDT) TEST VEHICLE

The following sections describe the construction of the LCDT including communication interfaces with the DUT and user PCs.

3.1 Architectural Overview

The EZ-USB FX2 controller/processor is instantiated as a sub component within the Low Cost Digital Tester (LCDT). The LCDT consists of a Mother Board (FPGA Based Controller/Processor) and a daughter board (containing DUT and its associated necessary circuitry). The objective of this DUT Controller/processor is to supply inputs to the EZ-USB FX2 Device and perform data processing on the outputs of the EZ-USB FX2. The LCDT communicates with a user controlled PC (Capture PC). The user interface is LAB-VIEW. It will send user specified commands to the mother board and receive information from the mother board. Please see Documents: “LCDT” and “General Tester” for further information concerning the LCDT functionality. The LCDT is connected to the EZ-USB FX2 DUT as shown in the following Block Diagram.

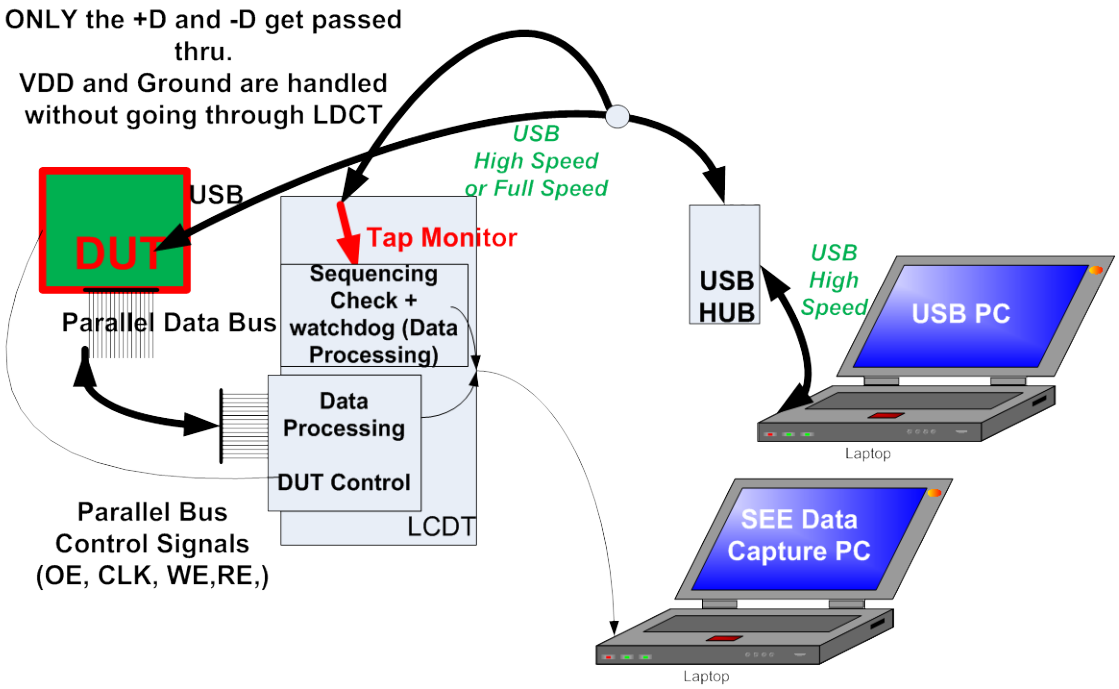

Figure 3. System Level Tester Architecture.

There are two PCs utilized in the test setup as illustrated in Figure 3. The capture PC is used to:

- Send commands to the LCDT (test parameters (read test or write test), start test,etc…) via RS232
- Receive SEU information from the LCDT via RS232

The USB PC is used solely for USB packet transfer to and from the DUT:

- Read Mode: The LCDT sends data to the DUT (via the DUT's parallel interface). The DUT transforms the parallel data to USB data packets including USB protocol packets to be sent to the USB PC. LCDT also monitors the DUT to PC USB D+,D- signals to check that the expected sequencing of packets are being sent and to determine if and when the DUT enters a lockup condition. Upon unexpected data or responses, the LCDT sends the information to the capture PC
- Write Mode: The PC sends data to the DUT via the USB connection. Prior to data packets being sent, the PC and DUT send a series of protocol packets. LCDT monitors the DUT to PC USB D+,D- signals to check that the expected sequencing of packets are being sent and to determine if and when the DUT enters a lockup condition. During data packets, DUT transforms the USB data to parallel data. The LCDT monitors the parallel output port of the DUT and verifies that the proper data is being received. Upon unexpected data or responses, the LCDT sends the information to the capture PC

3.1.1 I/O List and Definitions

Interface tables were supplied in the previous sections for all of the designs. The same I/O for each of the 2 DUTs are presented with respect to the LCDT in this section (see Table 1).

Table 1: I/O DUT1 I/O Table Shift Register, Memories, and Host PC Interface

Input Name	bits	Direction with respect to LCDT	Description
CLK	1	IN	100MHz input clock to tester. Tester will use several DCMs to synthesize the faster clocks required by the DUTs (200MHz WSR, 120MHz Counter, 120MHz DSP)
Reset	1	IN	Resets entire tester
TXRS232	1	OUT	RS232 output to PC: Command Echo and WSR Data
TX0RS232	1	OUT	RS232 output to PC: Counter Array Data
TX1RS232	1	OUT	RS232 output to PC: DSP Block Data
RX2RS422		IN	Command interface from PC to Tester
USB_DP	1	IN	USBD+ Serial bidirectional NRZ signal. Communication is between PC and DUT. Tester is tapped into the line in order to monitor protocol and data packets. Tester compares USBD+ to expected values. If an error occurs, capture PC is notified
USB_DN	1	IN	USBD- Serial bidirectional NRZ signal. Communication is between PC and DUT. Tester is tapped into the line in order to monitor protocol and data packets. Tester compares USBD- to expected values. If an error occurs, capture PC is notified
I_USB_IFCLK	1	IN	48MHz Clock from DUT

Table 1: I/O DUT1 I/O Table Shift Register, Memories, and Host PC Interface

Input Name	bits	Direction with respect to LCDT	Description
IO_USB_DATA	16	INOUT	Bi-directional parallel data bus DUT to LCDT
I_USB_CMD_DAT	1	IN	Indicates data on bus is a command (DUT to LCDT)
I_USB_RE	1	IN	Indicates DUT wants to read data from the LCDT
I_USB_WE	1	IN	Indicates DUT wants to write data to the LCDT
I_USB_OE_N	1	IN	Indicates that LCDT has control of bus during a read (OE is low). OE high – DUT has control over bus
O_USB_EMPTY_N	1	OUT	LCDT indicates that it doesn't have data
O_USB_FULL_N	1	OUT	LCDT indicates that it is full and data cannot be written to it

4. DUT TEST OBJECTIVES

The objectives of testing are to determine:

- Single Event Latchup (SEL) susceptibility
- Lock-up rates
- Data packet upset rates
- USB mode effects (High-speed versus Full Speed)
- There are two major tests:
- Read: LCDT feeds the DUT 16bits of data through its parallel port every clock cycle that the DUT signals that it is ready to receive data. Data speed is16bits at 48MHz. The speed will comply with USB 2.0 full or High speed transfer. The DUT converts the parallel data to USB serial NRZ data packets including supporting protocol packets. The USB data is sent from the DUT to the USB PC. USB DUT output is monitored by the LCDT.
- Write: PC feeds the DUT USB protocol and data packets. The DUT converts the USB data packets to 16-bit parallel data. LCDT reads the parallel DUT output port to verify correct data is sent. USB DUT output is monitored by the LCDT.

Each Read or Write test can be run in high or full speed mode. Only full speed mode will have the capability of USB monitoring within the LCDT. This means that full speed will have the capability to determine exactly what part of the protocol handshaking sequence the DUT and PC are operating in at all times. This provides enhanced visibility and will assist in post processing of SEE data. High speed testing is limited however it can report if the DUT is locked (via a timeout) or if data is corrupted. It is important to note that high-speed will not have the detailed information that full speed mode supplies (i.e. determining which state during protocol handshaking the DUT becomes locked)

4.1 SEL Testing

During every test, the DUT current is monitored. Fluctuations in current are recorded for further processing. If a current rise occurs, it is noted as a SEL. The DUT is tested after a SEL to determine if the SEL is a destructive event.

4.2 Running a Test with Full Speed Mode

The DUT will operate during a heavy ion test run. Parameters for the test (e.g. read or write) must be set before the DUT is brought out of reset. USB bits are roughly 83ns wide in full speed mode. The tester is capable of taping into the D+D- USB lines to verify proper sequencing. This provides enhanced visibility into the DUT during irradiation in order to decipher potential lockup states. Packet sequencing is in default mode (ON) during full speed mode.

4.3 Running a Test with High Speed Mode

The DUT will operate during a heavy ion test run. Parameters for the test (e.g. read or write) must be set before the DUT is brought out of reset. USB bits are roughly 2ns in length for High speed mode. The tester is not capable of taping into the D+D- USB lines to verify proper sequencing. Additional hardware such as a transceiver (mixed signal serial to parallel device), is required to perform the sequence monitoring for high-speed mode. Packet sequencing is (OFF) during high speed mode.

5. HEAVY ION TEST FACILITY AND TEST CONDITIONS

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 15 MeV/amu
Fluence: All tests will be run to 1 x 10^7 ions/cm^2 or until destructive or functional events occurred.

Table 2: LET Table

Ion	Energy (MEV/Nucleon)	LET (MeV*cm^2/mg) 0 °	LET (MeV*cm^2/mg) 45 °
He	15	0.5	1.5
Ne	15	2.8	3.96
Ar	15	8.5	12.6
Cu	15	17	27.9
Xe	15	52.7	75.09

Test Conditions:

Test Temperature:	Room Temperature
Operating Frequency:	High Speed and Full Speed USB 2.0 Protocol
Power Supply Voltage:	3.3v I/O and 1.5V Core.

The test setup at TAMU is shown in the following figures. Figure 4 shows the working end of the test cave at TAMU. The test samples are placed on the far side of the chamber. Diagnostics and control electronics are accessed remotely through cabling.

Figure 4. Texas A&M University (TAMU) Cyclotron Test Cave

Figure 5 and Figure 6 show the USB Microcontroller in the test configuration along with the LCDTv3. Figure 7 and Figure 8 show the USB Hub test configuration.

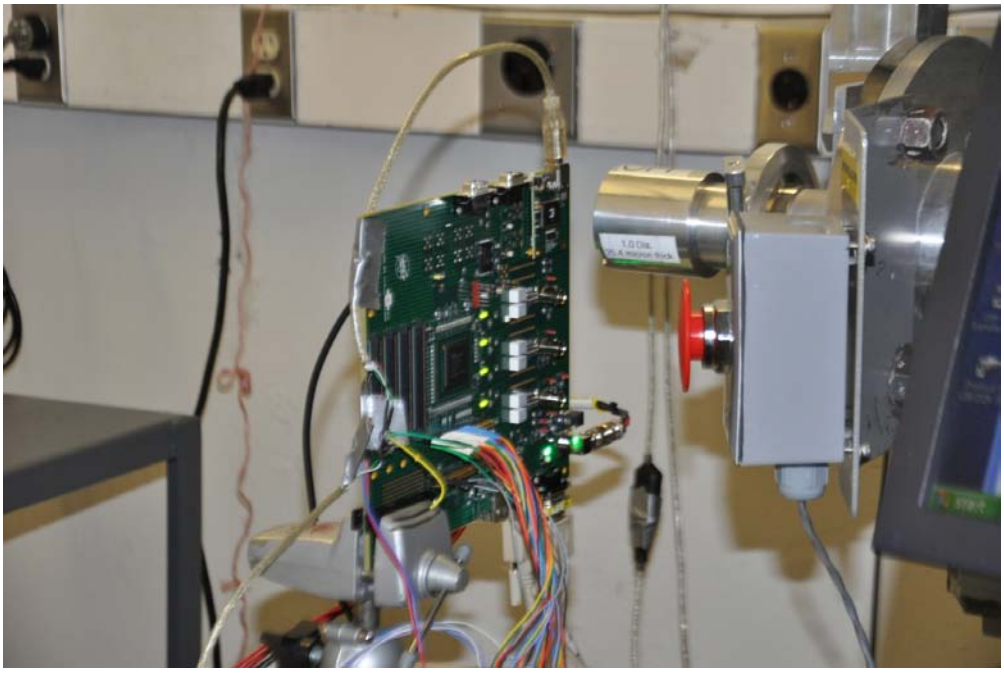

Figure 5. Low Cost Digital Tester v3 (LCDTv3) focusing on USB microcontroller

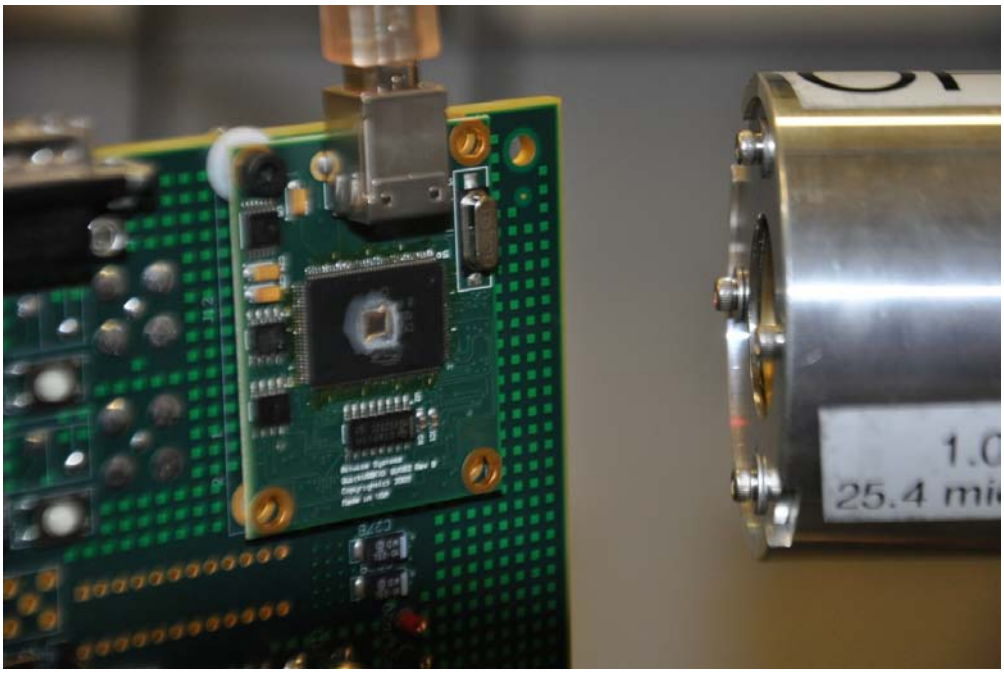

Figure 6. LCDTv3) focusing on USB microcontroller – closeup.

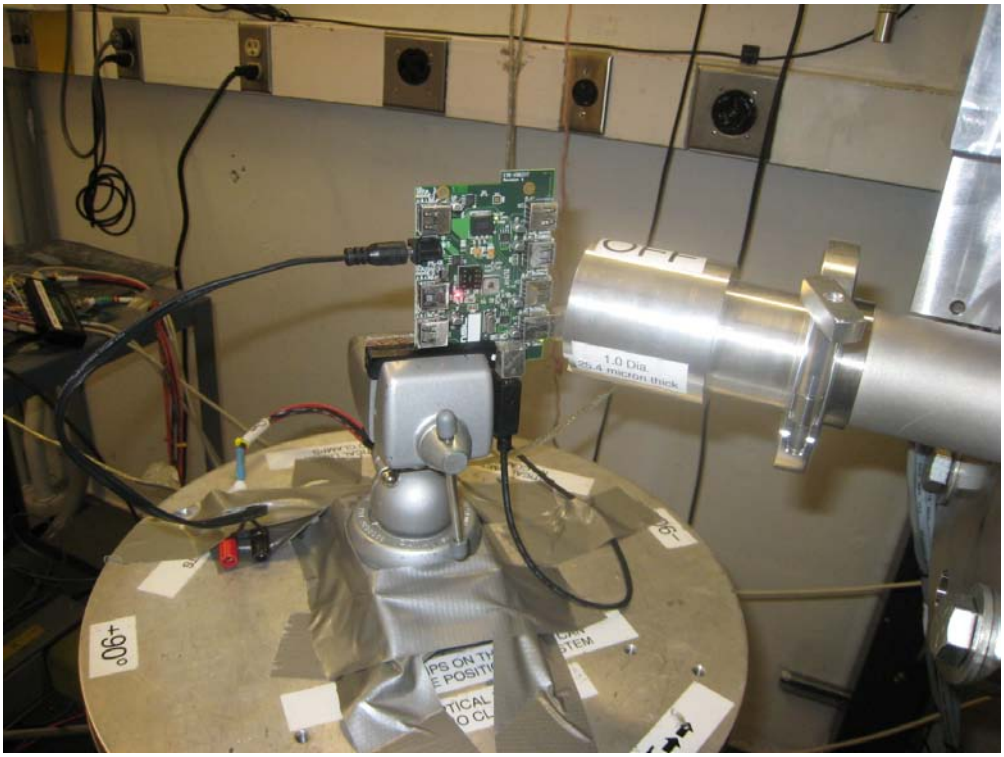

Figure 7. LCDTv3 with USB Hub mounted on facility pedestal.

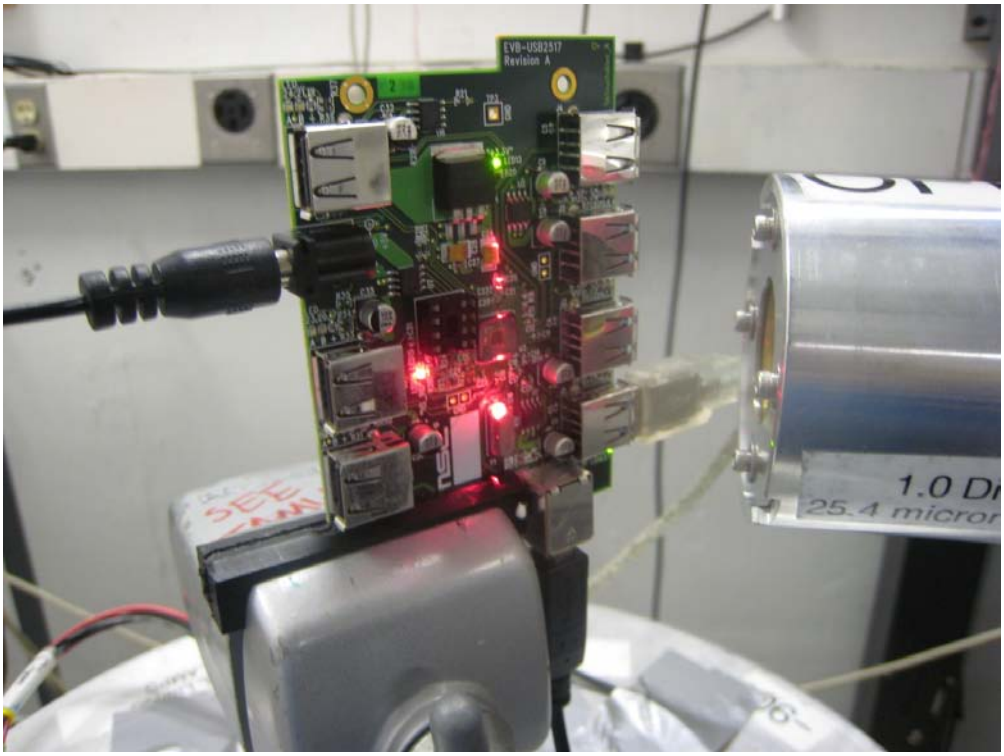

Figure 8. LCDTv3, focusing on USB Hub

5.1 Error Message Descriptions and Formats for USB Controller and HUB Testing

The following section identifies the types of errors being monitored by the LCDTv3.

Write Phase Data Error: The USB controller received incorrect/corrupted data from the host. Observed from controller's position. Valid only for Data packets.

Write Phase Data Error message format

Field name	Bit Range	Field Value
Time Stamp	183 downto 152	Timer value in increments of 20nS
Error Count	151 downto 136	Write Phase Data Error count
Error Type Indicator	135 downto 128	x"01" for Write Phase Data Error
Data Packet Value	127 downto 0	Value of Data Packet in error

Sequence Error Message: Read or Write Mode – Observed by Tester on the transmission lines. A packet in the communication sequence is corrupted or missing. Valid on any packet.

Sequence Error message format

Field name	Bit Range	Field Value
Time Stamp	183 downto 152	Timer value in increments of 20nS
Error Count	151 downto 136	Read Phase Sequence Error count
Error Type Indicator	135 downto 128	x"02" for Read Phase Sequence Error
Packet Type History	127 downto 64	16 previous 4-bit packet type codes (see table)
Data Packet Value	63 downto 0	Value of Data Packet in error - 64 bits of MSB

Read Phase Data Error: The Host controller received incorrect/corrupted data from the controller. Observed by tester on the transmission line. Valid only for Data packet.

Read Phase Data Error message format

Field name	Bit Range	Field Value
Time Stamp	183 downto 152	Timer value in increments of 20nS
Error Count	151 downto 136	Read Phase Data Error count
Error Type Indicator	135 downto 128	x"04" for Read Phase Data Error
Data Packet Value	127 downto 0	Value of Data Packet in error

USB Host Packet Timeout: Packet from Host not observed on transmission line within programmable timeout time (tested with 2ms timeout).

USB Host Packet Timeout message format

Field name	Bit Range	Field Value
Time Stamp	183 downto 152	Timer value in increments of 20nS
Error Count	151 downto 136	USB Host Packet Timeout count
Error Type Indicator	135 downto 128	x"06" for USB Host Packet Timeout
Packet Type History	127 downto 64	16 previous 4-bit packet type codes (see table)
Data Packet Value	63 downto 0	Value of Data Packet in error - 64 bits of MSB

End Point Packet Timeout: Packet from Controller not observed on transmission line within programmable timeout time (tested with 2ms timeout).

End Point Packet Timeout message format

Field name	Bit Range	Field Value
Time Stamp	183 downto 152	Timer value in increments of 20nS
Error Count	151 downto 136	EP0 or EP6 Packet Timeout count
Error Type Indicator	135 downto 128	x"07" for EP0 Packet Timeout
		x"08" for EP6 Packet Timeout
		x"0D" for EP2 Packet Timeout
Packet Type History	127 downto 64	16 previous 4-bit packet type codes (see table)
Data Packet Value	63 downto 0	Value of Data Packet in error - 64 bits of MSB

Parallel CTL Signal Timeout: Parallel USB controller port control signal is not observed within programmable timeout time (tested with 40ms timeout).

Parallel CTL Signal Timeout message format

Field name	Bit Range	Field Value
Time Stamp	183 downto 152	Timer value in increments of 20nS
Error Count	151 downto 136	WE, RE, OE, or CLK Timeout count
Error Type Indicator	135 downto 128	x"09" for WE Timeout
		x"0A" for RE Timeout
		x"0B" for OE Timeout
		x"0C" for CLK Timeout
Packet Type History	127 downto 64	16 previous 4-bit packet type codes (see table)
Data Packet Value	63 downto 0	Value of Data Packet in error - 64 bits of MSB

Packet Type Codes - Used in Packet Type History field of error messages

Code Description	Code Value (4 bits : hex format)
Setup Token	x"D"
"OUT" Token	x"1"
"IN" Token	x"9"
"Start of Frame" Token	x"5"
DATA0	x"3"
DATA1	x"B"
ACK	x"2"
NAK	x"A"

5.2 Microcontroller Test Results for Heavy Ions

A table of the test findings – by shot number may be found in the Appendix A. The discussion herein is a summary of that data.

Testing of the USB Controller was complicated by high current conditions brought about by the exposure to heavy ions. These conditions were found at all ions and all LET values (down to an LET of 1.3 MeV•cm^2/mg). No threshold was found. Figure 9 shows the cross section of the DUT response during exposure.

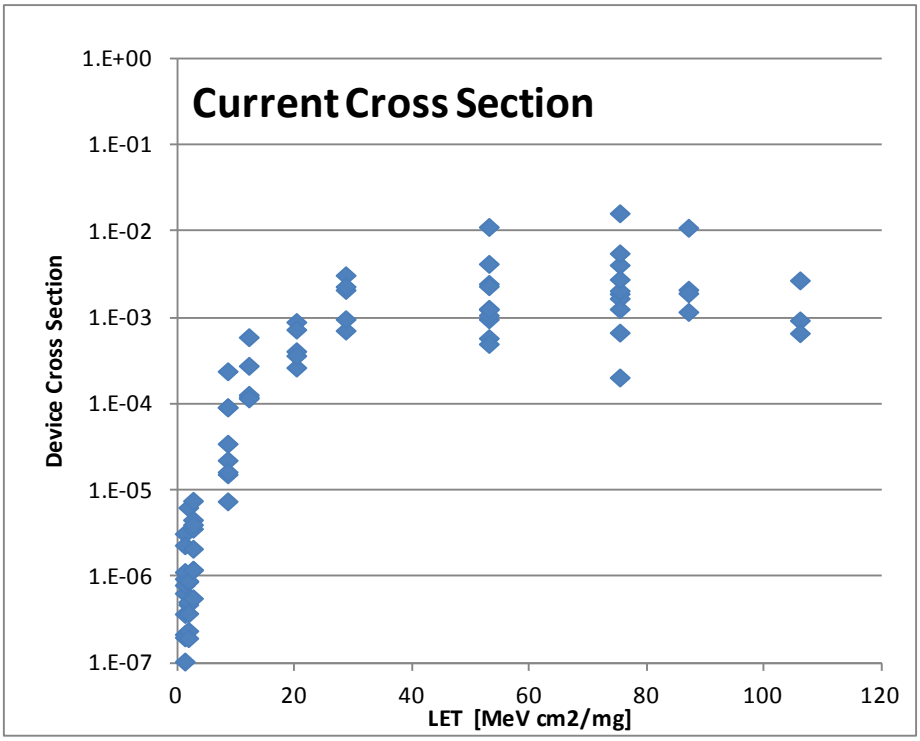

Figure 9. Microcontroller device cross section to high current response.

Figure 10 shows the corresponding currents which were measured during exposure. The data does show large deviations – but that is to be expected because of the low fluences required to force the device into this mode. However, the general trend is that as the LET increases, the current response also increases.

In each case, a power-on-reset (POR) was required to reinitialize the DUT to functionality. While no damage was identified from the high current condition, it was current limited and the POR was required.

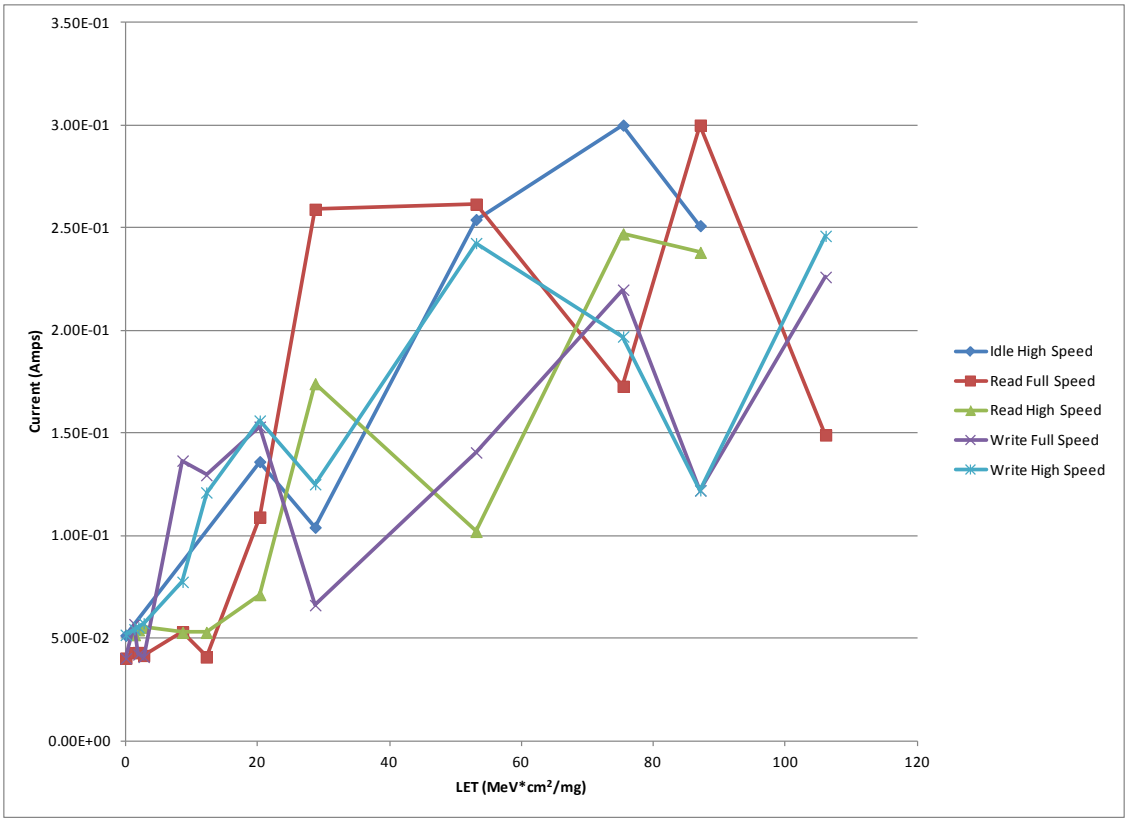

Figure 10. Microcontroller current response as a function of LET.

While the device was functioning, errors were monitored (see Section 5.1). Figure 11 shows the device cross section for all errors recorded. Again, this data is somewhat problematic since at no time did the DUT remain functional for the entire exposure of 1E7 ions. This may tend to impact data at high LETs since the high current conditions took place at low fluence levels.

The total errors monitored were broken down into discrete error patterns. For the test, errors were recorded in the Read Phase (Figure 12), Read Enable (Figure 13) and Write Enable (Figure 14) functions.

Again, it should be stressed that the DUT going into high current conditions forced the exposure to stop premature of the desired 1E7 ion fluence. As such, all errors may not have been identified for the device, or in sufficient quantity to provide the best statistics.

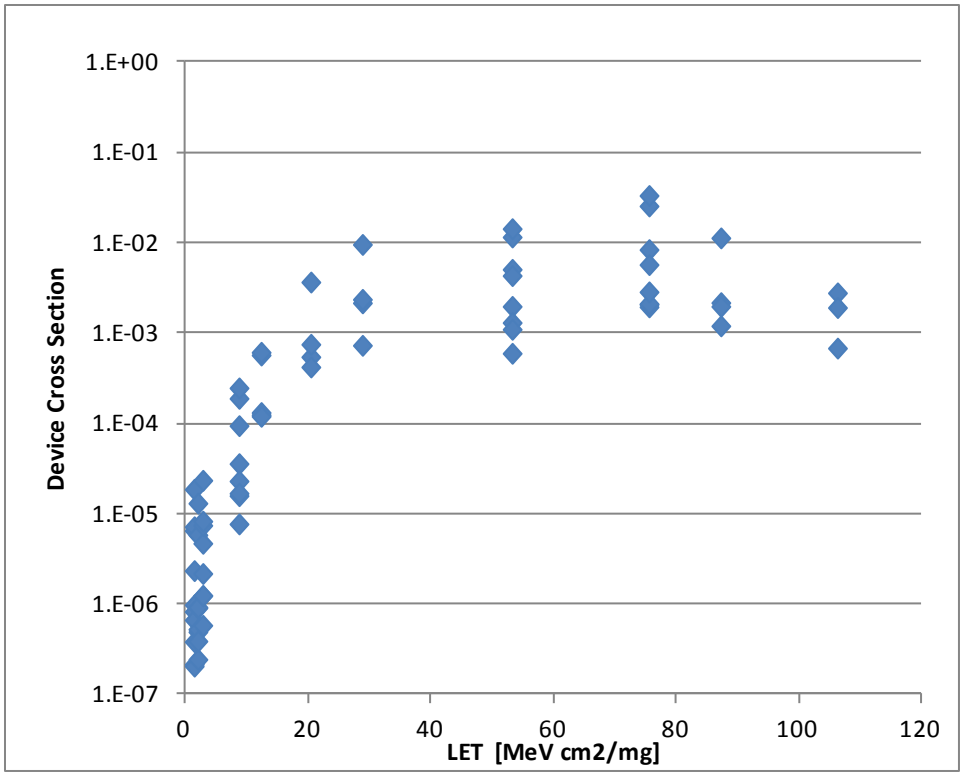

Figure 11. Microcontroller Heavy Ion response to all errors recorded.

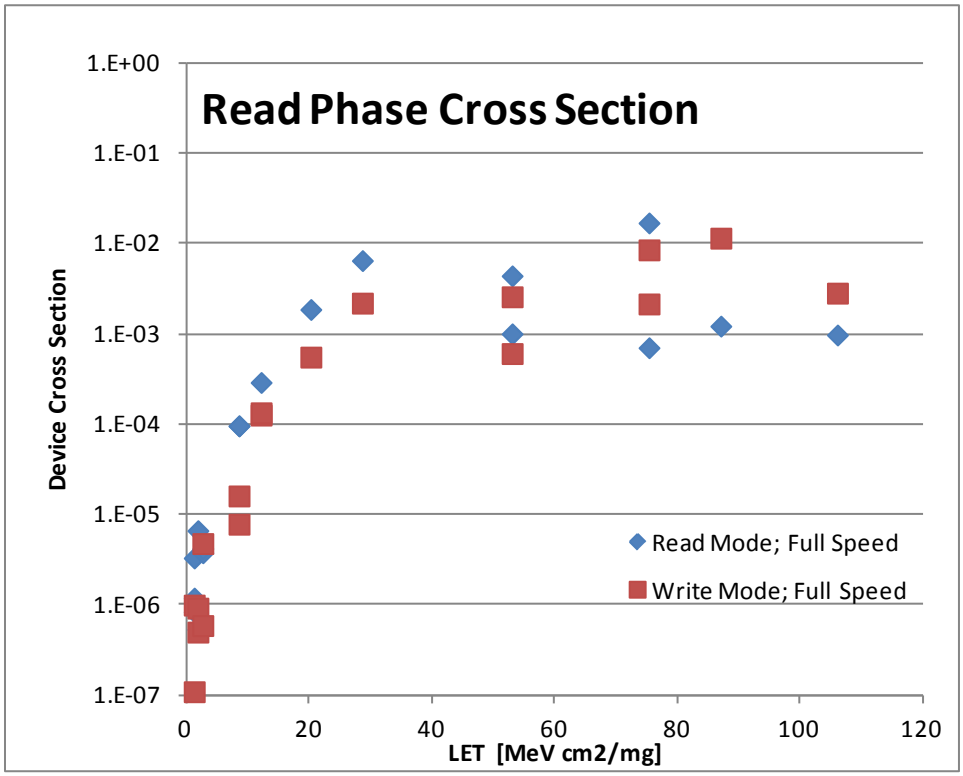

Figure 12. Microcontroller cross section for Read Phase errors.

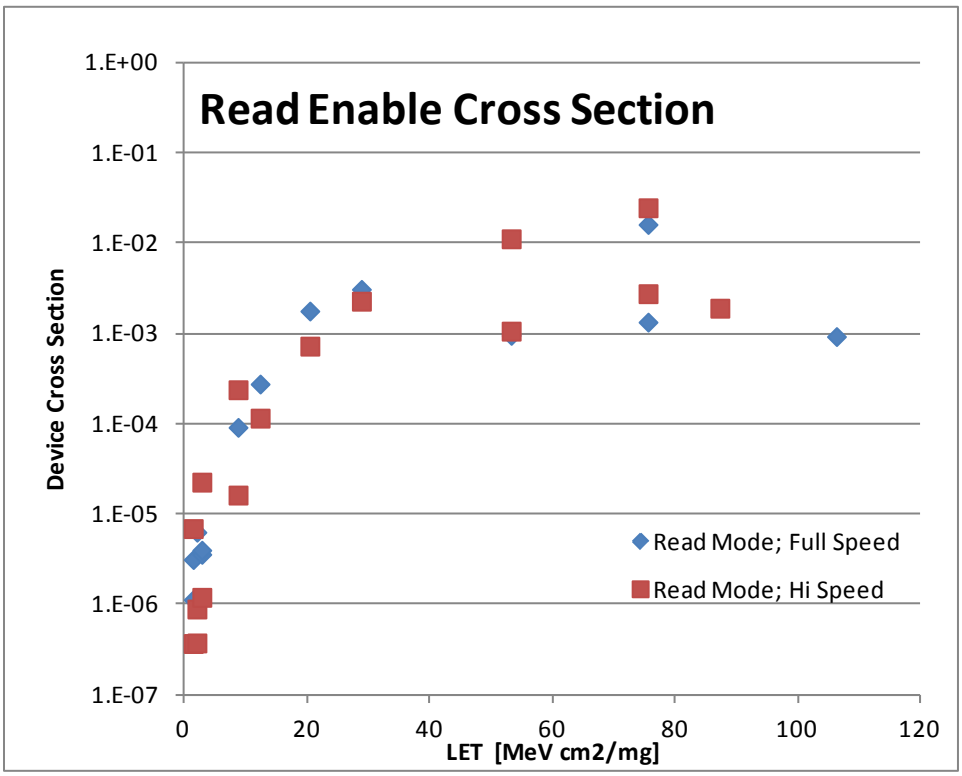

Figure 13. Microcontroller cross section for Read Enable errors.

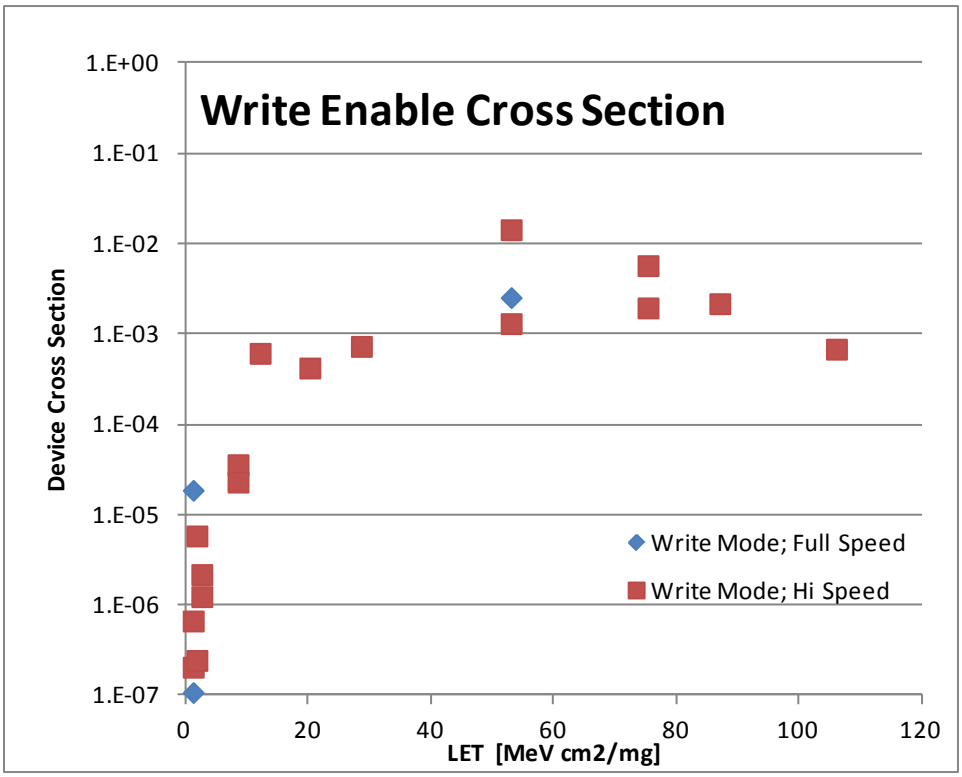

Figure 14. Microcontroller cross section for Write Enable errors.

5.3 USB Hub Test Results for Heavy Ions

A table of the test findings – by shot number may be found in the Appendix B. The discussion herein is a summary of that data.

Testing of the USB Hub was complicated by high current conditions brought about by the exposure to heavy ions. These conditions were found at all ions and all LET values (down to an LET of 1.3 MeV•cm^2/mg). No threshold was found. Figure 15 shows the cross section of the DUT response during exposure.

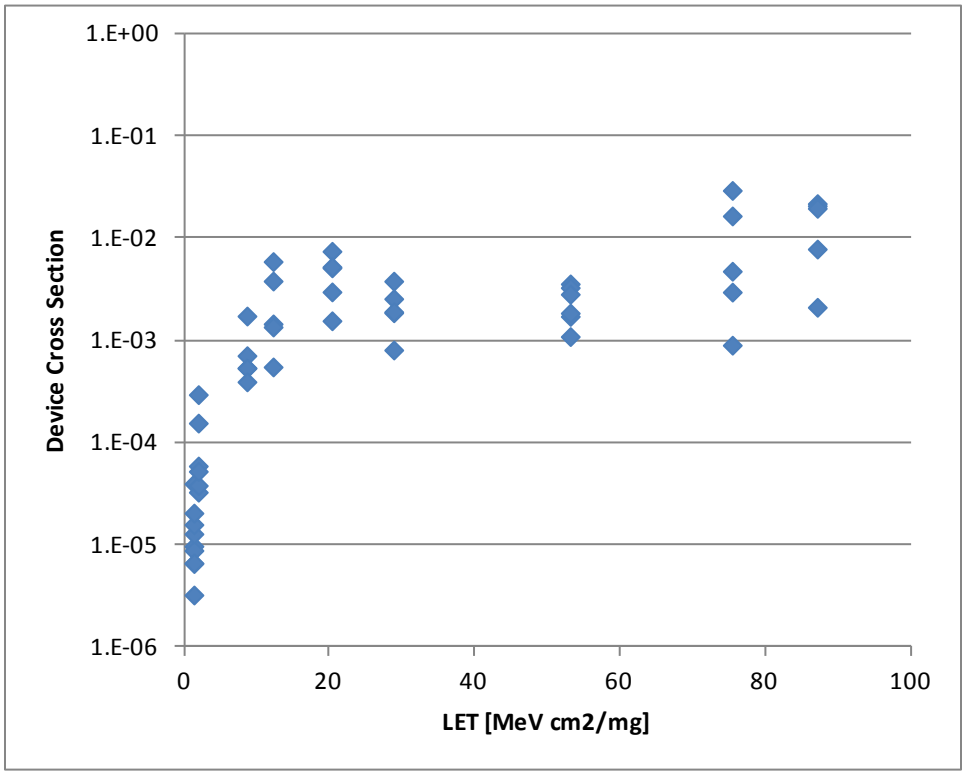

Figure 15. Hub device cross section to high current response.

Figure 16 shows the corresponding currents which were measured during exposure. In each case, a power-on-reset (POR) was required to reinitialize the DUT to functionality. While no damage was identified from the high current condition, it was current limited and the POR was required.

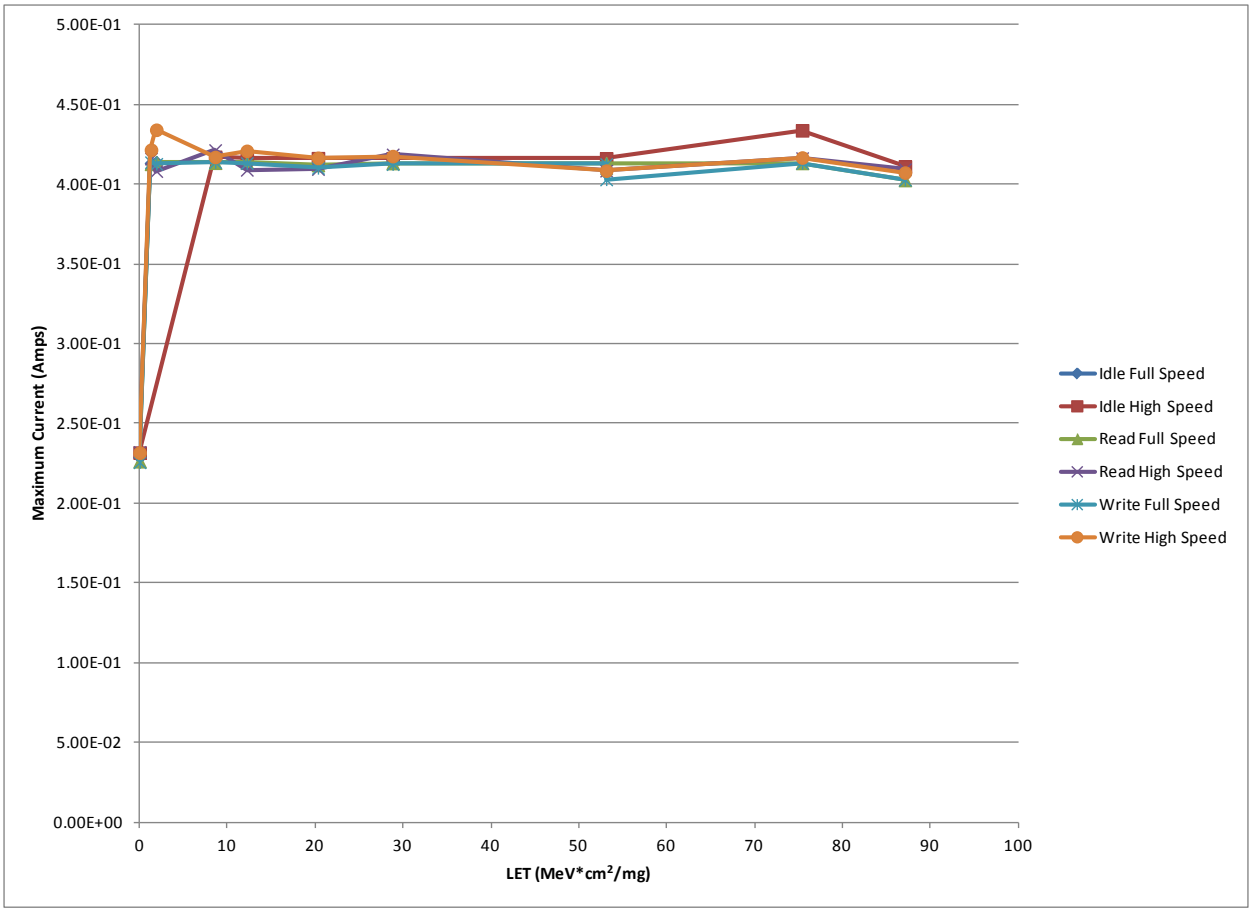

Figure 16. Hub current response as a function of LET.

While the device was functioning, errors were monitored (see Section 5.1). Figure 17 shows the device cross section for all errors recorded. Again, this data is somewhat problematic since at no time did the DUT remain functional for the entire exposure of 1E7 ions. This may tend to impact data at high LETs since the high current conditions took place at low fluence levels.

The total errors monitored were broken down into discrete error patterns.

USB Host Packet Timeout	Figure 18
Write Enable Timeout	Figure 19
Read Enable Timeout	Figure 20
Output Enable Timeout	Figure 21
Clock Timeout	Figure 22

Again, it should be stressed that the DUT going into high current conditions forced the exposure to stop premature of the desired 1E7 ion fluence. As such, all errors may not have been identified for the device, or in sufficient quantity to provide the best statistics.

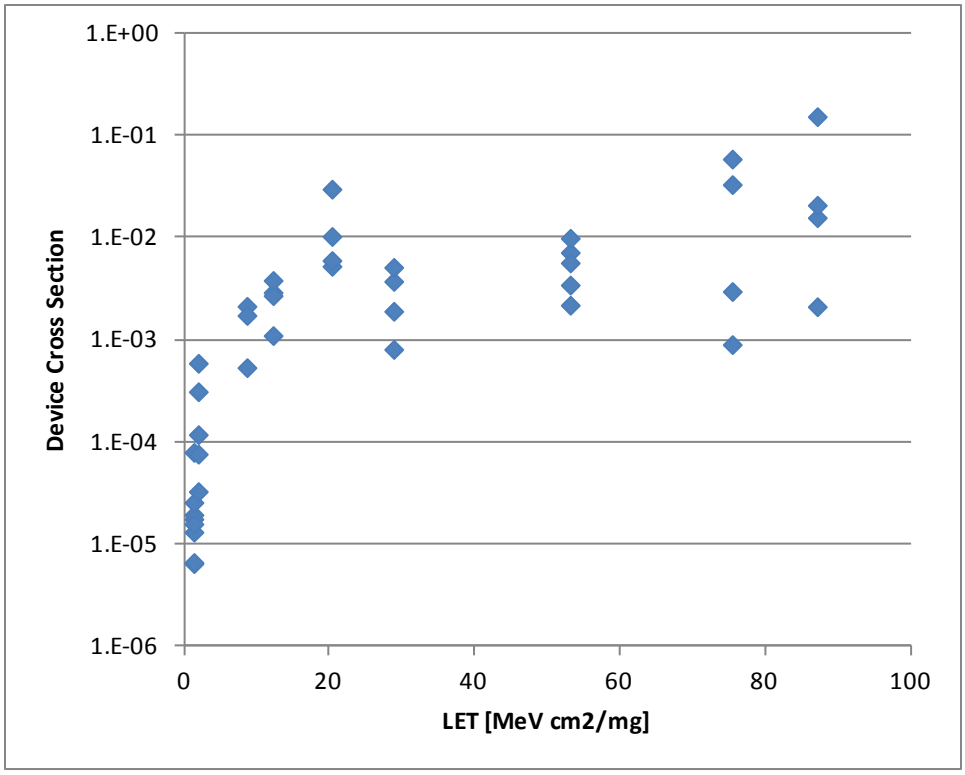

Figure 17. Hub Heavy Ion response to all errors recorded.

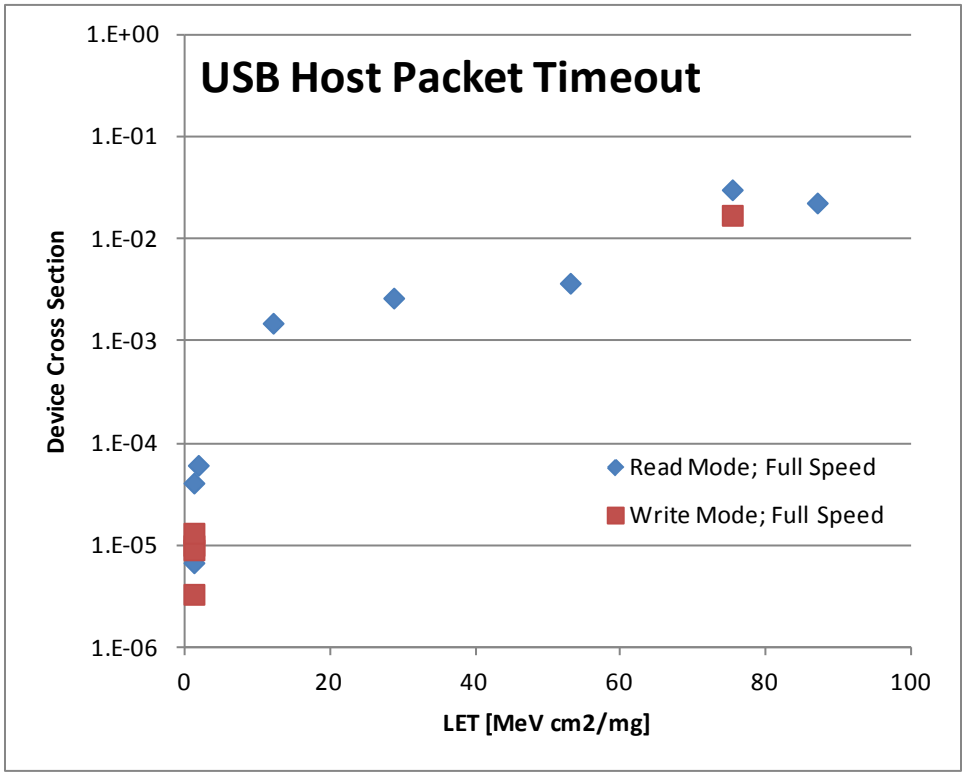

Figure 18. Hub device cross section with USB Host Packet Timeout Errors.

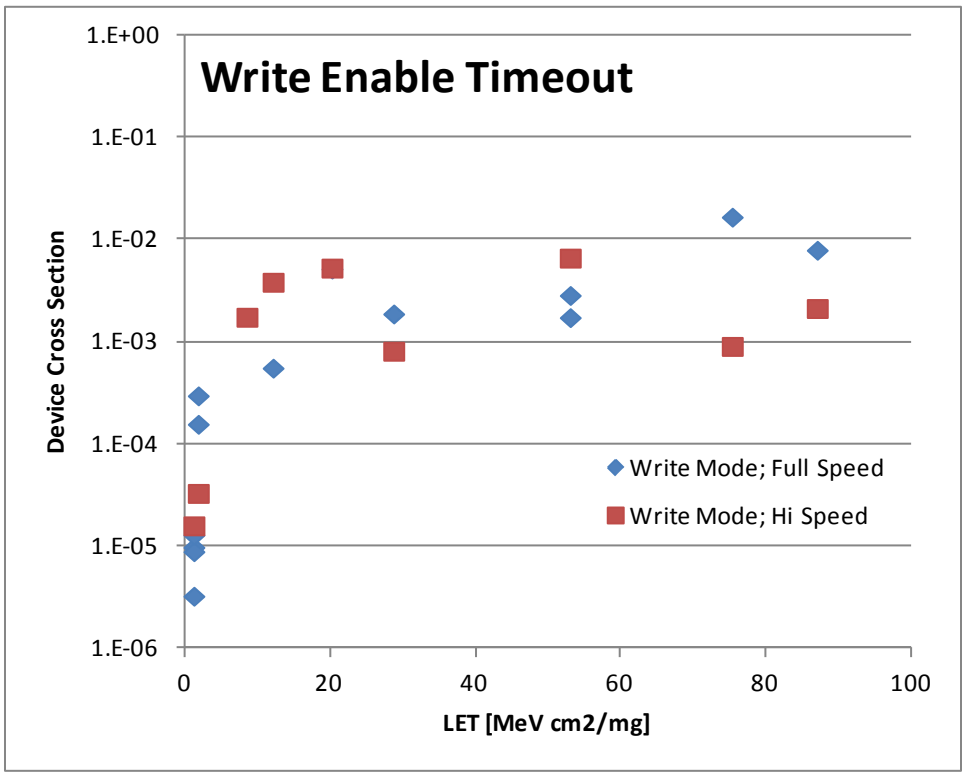

Figure 19. Hub device cross section with Write Enable Errors.

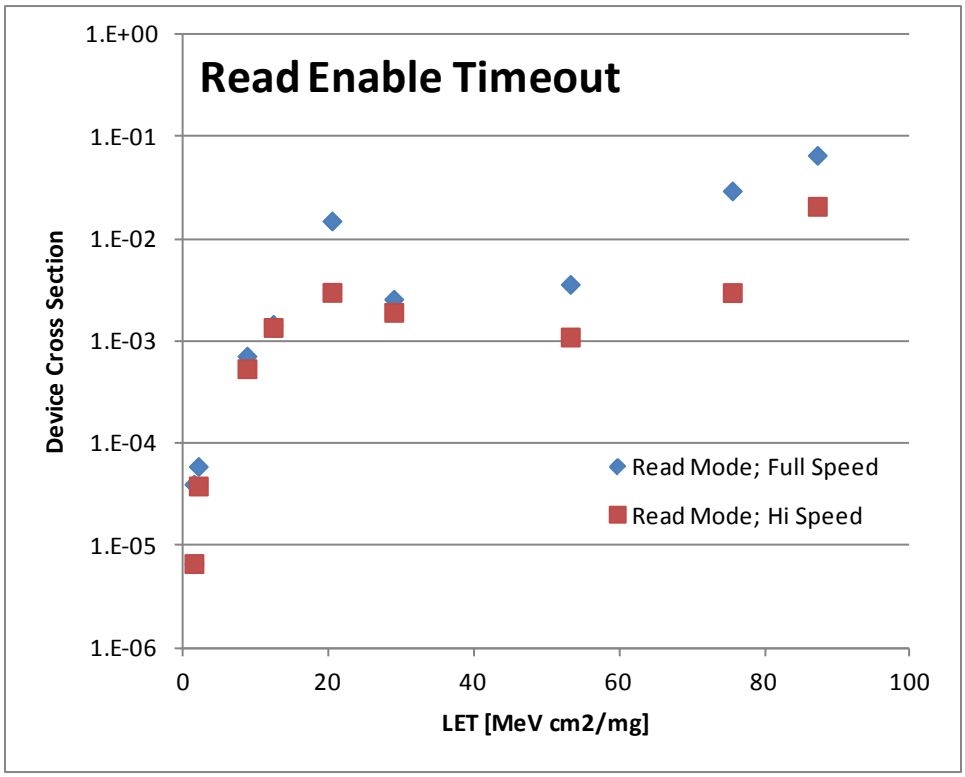

Figure 20. Hub device cross section with Read Enable Errors.

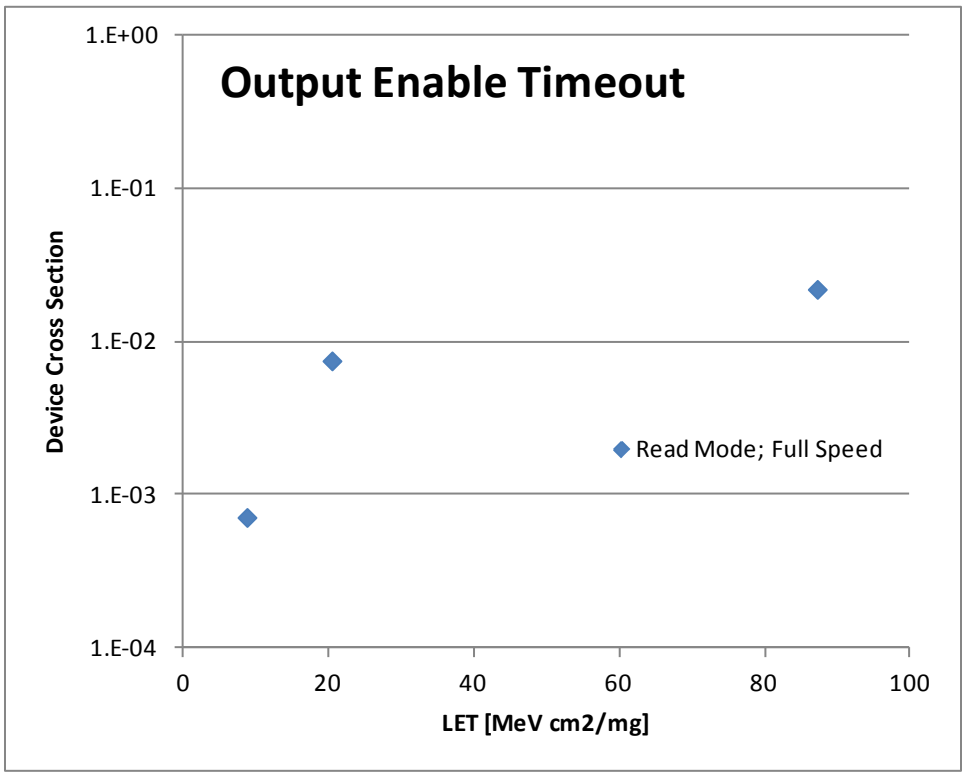

Figure 21. Hub device cross section with Output Enable Errors.

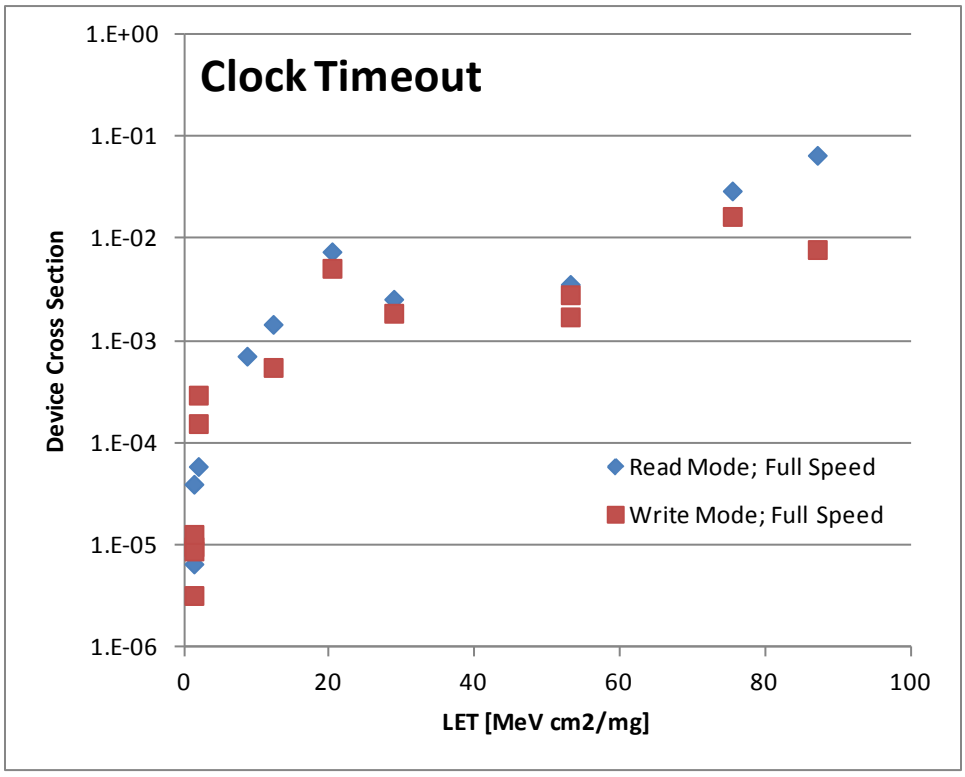

Figure 22. Hub device cross section with Clock Timeout Errors.

6. RECOMMENDATIONS

Both the USB Microcontroller and the USB Hub experienced non-destructive high current latchup-like conditions which required power-on-reset to re-establish functionality. This condition severely limited the ability of the test set to monitor all error modes with sufficient statistics (1E7 ions was not reached on any exposure). At high LET values, the exposure time/fluence was very low due to the rapid onset of the high current condition.

Should this device be used for space flight applications, it is recommended that active monitoring of the devices be supplied such that the device(s) can be re-initialized via a power-on-reset (POR). Given the frequency of the required POR, it is recommended that a set of electrical tests should be conducted to determine the long term reliability impact of multiple high current events on the device (and any surrounding circuitry) which may impact the life of the device.