Heavy Ion SEE Test Report for the Samsung 4Gbit NAND Flash Memory for MMS

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I. Introduction

This study was undertaken to determine and compare the susceptibilities of 4 Gbit NAND Flash memories from Samsung to destructive and nondestructive single-event effects (SEE) for the NASA MMS mission. The devices were monitored for SEUs, errors from individual cells, for SEFIs, errors arising in the control logic, and for destructive events, including latchup, induced by exposing them to a heavy ion beam at the Texas A&M University Cyclotron.

II. Devices Tested

We tested a total of fourteen Samsung parts, from four different date codes (part number K9F4G08U0A-PCB0, Lot Date Codes (LDC) 0840, 0843, 0846, 0901). We began with eight parts from each date code delidded and fully operational on the bench at Goddard, that were shipped to TAMU. However, not all of them worked properly at TAMU. What we actually used was three parts from LDC 0840, five parts from LDC 0843, two parts from LDC 0846, and four parts from LDC 0901. The parts have 512Mx8 organization with large blocks. That is, the blocks are 128Kx8, with 64 pages/block. Each page is nominally 2Kx8, but they also have 64 redundant columns, which makes the total page size 2112x8. NAND flash normally has some bad blocks which can be screened off. The specification is that no more than 80 of the 4096 blocks will be bad. In our experience, the parts almost always have a few bad blocks, but it is usually a single digit number. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility.

The device technology is 63 nm minimum feature size CMOS NAND Flash memory. All the parts are single die, SLC (single level cells). The chips came in a 48-pin TSOP package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface.

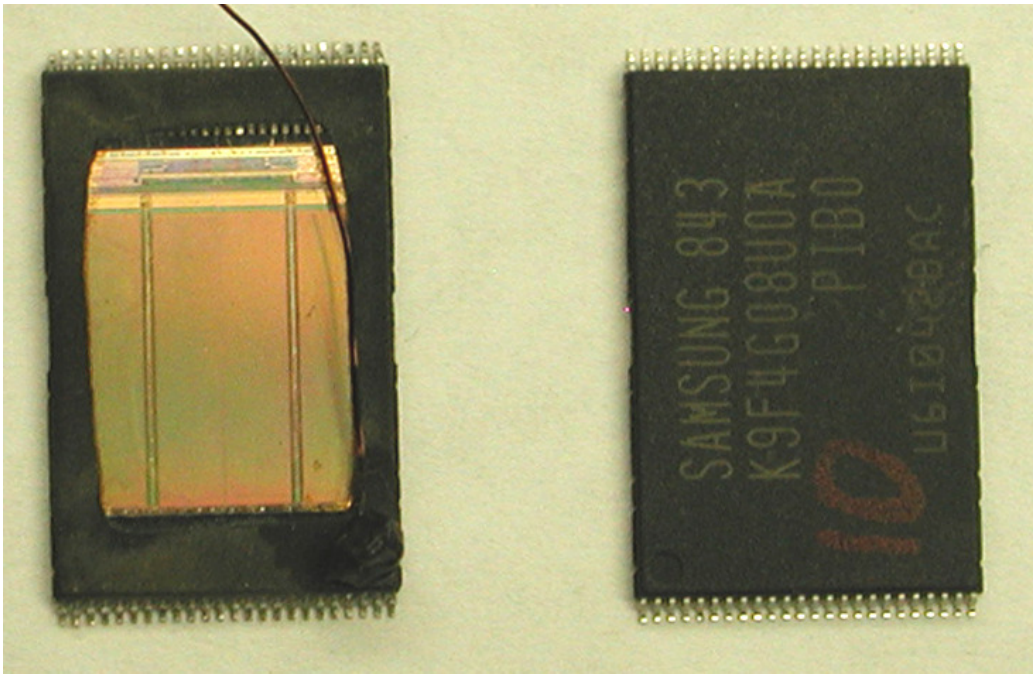

Fig. 1. Photos of die

III. Test Facilities

Facility: Texas A&M University Cyclotron
Flux: (5 x 10^3 to 1. x 10^5 particles/cm^2/s).
Fluence: All tests were run to 1E3 to 1E8 p/cm^2, or until destructive or functional events occurred.

Table I: Ions/Energies and LET for this test

TAMU Ions	Energy/ AMU	Energy (MeV)	Approx. LET on die (MeV•cm^2/mg)	Angle	Effective LET
Ne	15	300	2.7	0, 45	2.8, 3.9
Ar	15	600	8.4	0,45	8.4, 11.8
Kr	15	1260	30.1	0, 45	29.3, 41
Xe	15	1965	54.8	0, 45	53.9, 75
Au	15	2955	87.5	0	87.5

IV. Test Conditions

Test Temperature: Room Temperature for SEU, 70° C for SEL
Operating Frequency: (0-40 MHz).
Power Supply Voltage: (3.3V for SEU, 3.6V (3.3+10%) for SEL). Standard test methods for SEU testing (e.g., ASTM 1192) call for testing at nominal voltage less 10%, because SEU in standard volatile memories is caused by voltages being pulled down. However, flash memories are designed to retain information even at zero volts, so the upset mechanisms are clearly different, here. In addition, we are also looking for control logic errors, which are thought to be due to things turning on when they are not supposed to be on. Reduced voltage would cause an underestimate of the rate for these events. Therefore, we used nominal voltage, 3.3 V, in all tests except latchup tests, which were done at 3.6 V, and also at elevated temperature.

V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Test patterns included all 0's, all 1's, checkerboard and inverse checkerboard. In general, all zeroes is the worst-case condition for single bit errors. For a zero, the floating gate is fully charged with electrons. An ion can have the effect of introducing positive charge, which may be enough to cause a zero-to-one error. However, a checkerboard pattern (AA) was used in most of the testing because errors in the control circuitry can cause errors of both polarities. One-to-zero errors are an indication that the errors are coming from the control circuits. Between exposures, all patterns can used to exercise the DUT, to verify that it was still fully functional. However, all patterns are not used on every shot, just because it is time consuming to do so. The maximum clock frequency for these devices was 40 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors. In this

mode, the number of static bit errors is determined by reading the memory again, after the beam is turned off.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. In this mode, the words that are read are compared to an "expected" pattern, which is actually the complement of the stored pattern. For this reason, every word is erased, as if it were in error. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.

6) Latchup testing was conducted at 70° C, and 3.6 V. It was expected that high voltage, dynamic test modes would be most likely to result in latchup, so these were emphasized in the latchup testing.

7) In this set of experiments, we have attempted to look at angular effects, which may include multiple bits grazed by the same ion, and other effects due to charge sharing by multiple nodes in the control logic. This test was done with at 45 degrees, which was close to the maximum possible angle, because the socket would have blocked the beam at angles much higher. Generally, the error rate was slightly higher at high angles, so some tests were done only at high angle, but most tests were duplicated at normal incidence.

The Block diagram for control of the DUT is shown in Figure 2. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the flash is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for over-current conditions and shuts down power to the DUT if such conditions are detected.

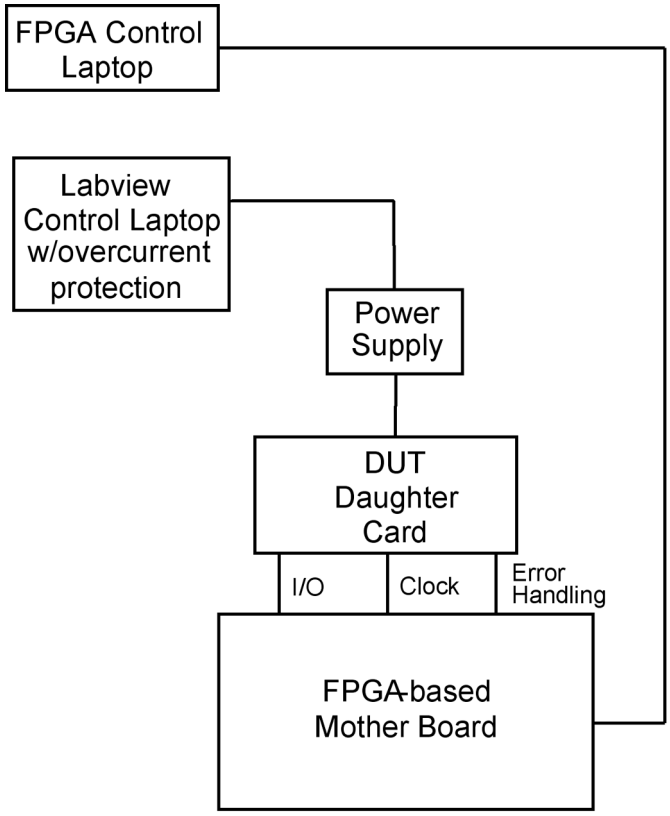

Figure 2. Overall Block Diagram for the testing of the NAND Flash.

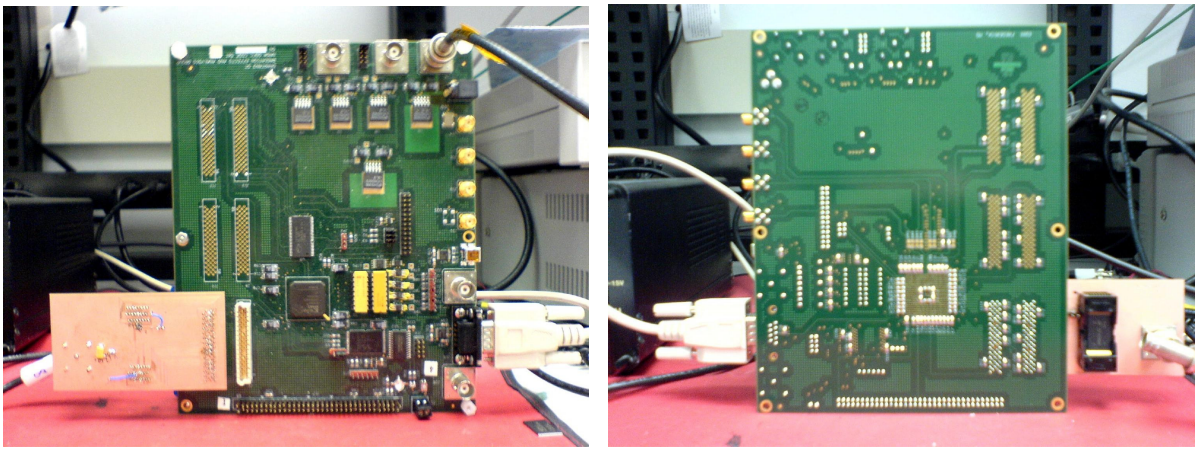

Fig. 3. Front and back views of motherboard and daughterboard, with DUT.

VI. Results

During testing, the DUTs were irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam, or at 45 degrees. The errors observed in static SEU testing are shown in Fig. 4, with no bias applied. The 45 degree data is plotted at the effective LET (LET/cos θ). This is done so that one can distinguish between the normal incidence shots and the 45 degree shots. It is <u>not</u> done because effective LET is expected to be a useful concept for other reasons.

Even for the static unbiased case, bit errors and one SEFI (LDC 0843) and one destructive failure (LDC 0840) were observed. The SEFI, which occurred with Xe ions incident at 45 degrees, was that blocks 0-15 were completely corrupted. The stored pattern (checkerboard, AA) was replaced with all ones (FF). Cycling power did not correct the errors, but the DUT was erased and rewritten successfully before the next shot. The destructive failure, which occurred with Au ions at normal incidence, was the failure of the erase circuit—the part still worked in read mode, but the pattern could not be altered. The failure of the erase function was probably due to damage to the charge pump, which was surprising only because the charge pump was unbiased. There does not appear to be any gross difference between any of the LDCs, in Fig 4. However, we were not able to take multiple shots at any test condition, in general, because of the need to repeat everything for the four different date codes. Therefore, the statistical confidence comes from the fact that the date codes give consistent results, and not from the fact that there is a lot of data for each date code. We believe the probability of errors in the control circuits is increased at high angles because more charge is generated close to the surface and over a wider area, and, therefore, closer to multiple active device regions. That is, charge sharing between multiple sensitive nodes is increased, compared to an exposure at normal incidence. Because the DUT was not actively exercised during the static exposures, we could not determine exactly when a SEFI or destructive failure occurred, so cross sections are approximate for these error modes. Here and in the following discussion, bit errors are taken to be single bits, which are flipped, as a result of the interaction with incident ions, normally from zero to one. We do not have the physical to logical address mapping, which would allow us to look for

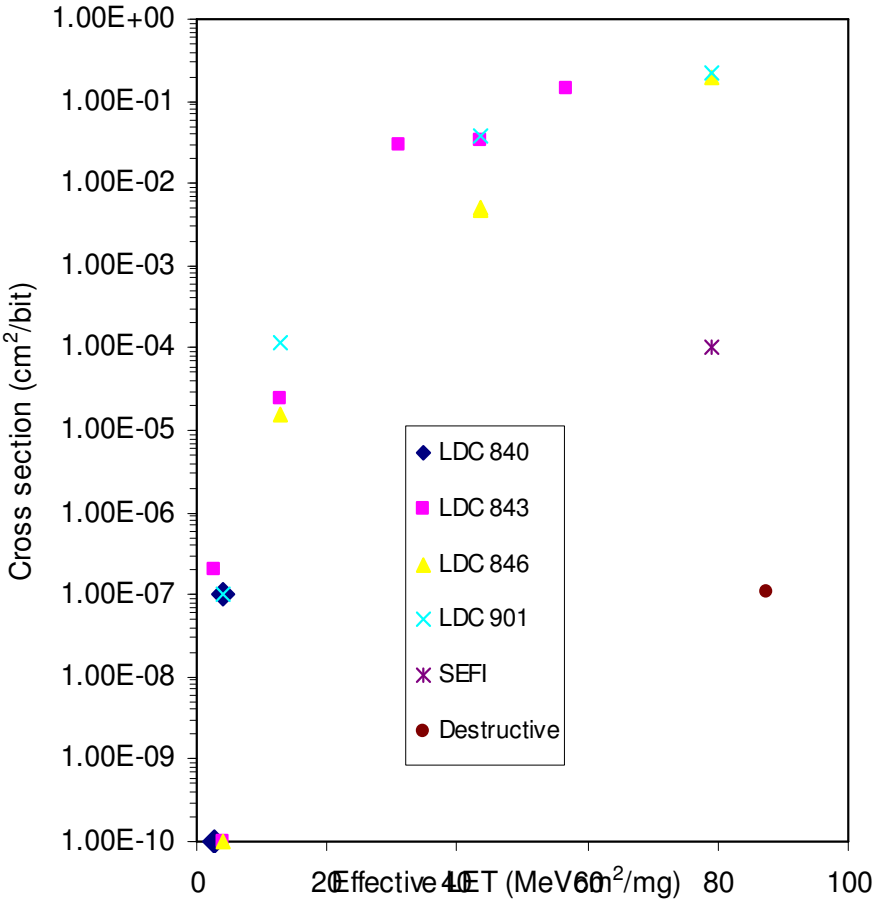

Fig. 4. Results in static, unbiased test mode.

multiple bit errors (error clusters) for these parts. However, in the overwhelming majority of cases of bit errors, there is only one error in a page, or one error in an entire block, which makes it extremely unlikely that there will be multiple bit cells upset from a single ion. This result is consistent with previously published results on the upset mechanism in flash memory—an ion passing through a floating gate creates a dense charge column, which creates a conducting path between the gate and substrate, which allows charge to leak off the floating gate. Since the ion only hits one gate at normal incidence, only one bit is affected. This situation is far different from that in volatile memories, where charge generated in the Si substrate can be shared across multiple nodes. Here and in the following sections, the only apparent multiple bit errors are due to errors in the control logic, for example, cases where an entire page or a block (or a large part of one) upsets simultaneously. These page and block errors are attributed to errors in the control logic, rather than to the individual bit cells. These are counted as SEFIs (Single Event Functional Interrupt). In general, a SEFI is any event where the entire DUT, or a large part of it, stops working, presumably from an interaction with a single ion.

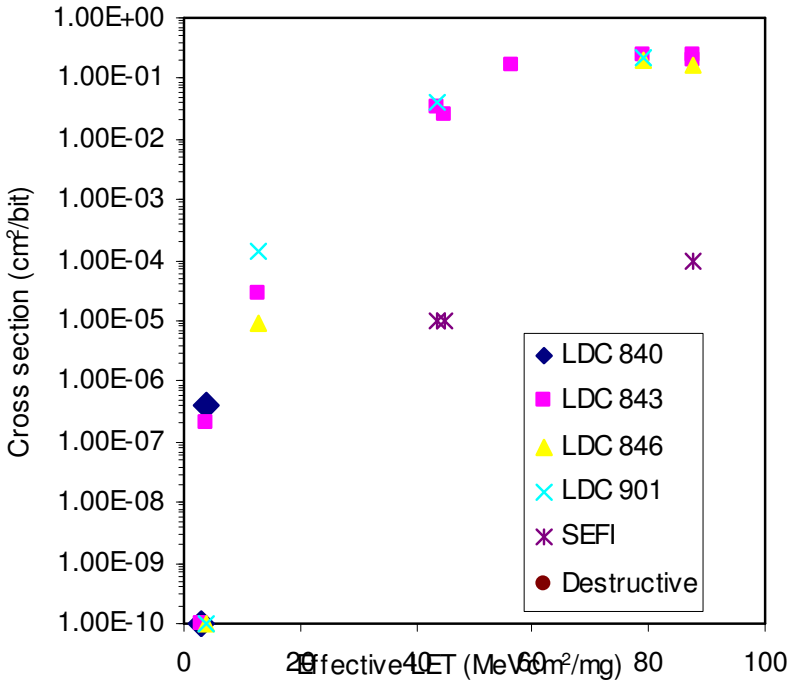

Fig. 5. Results for static mode, with bias applied.

The results for static mode with bias applied are shown in Fig. 5. The main effect is single bit upsets, along with three SEFIs, but no destructive events. The first SEFI, with Au ions at normal incidence (LDC 901) had 2400 five-bit errors after a power cycle. These were reset, and the part was used on the next shot. The other two SEFIs were both with Kr ions at 45 degree incidence (LDCs 0843 and 0846), with virtually the entire memory affected. Both parts largely recovered after a power cycle. The LDC 0843 part had 2559 bit upsets, which reset normally. The LDC 0846 part reported 377 remaining errors, but the error messages themselves appeared to have been corrupted, so the significance of the number is unclear, at best. However, the part reset properly, and was used on the next shot.

For the Dynamic Read condition, the parts showed exhibited transient read errors in addition to the bit errors, which are plotted in Fig. 6. In this mode, the DUT reads continuously with the beam on. The significance of the transient errors is not always completely clear, because the entire memory is read multiple times, which means static errors will be read multiple times. In addition there are errors due to transient noise in the read circuit or the control logic. The static errors are bit errors read after the beam is turned off. In this test mode, there were two SEFIs and no destructive events. One was with Au ions at normal incidence (LDC 0843), and the other was a page error with Kr ions at 45 degree incidence (LDC 0843). In both cases, the part reset properly, and was used on the next shot.

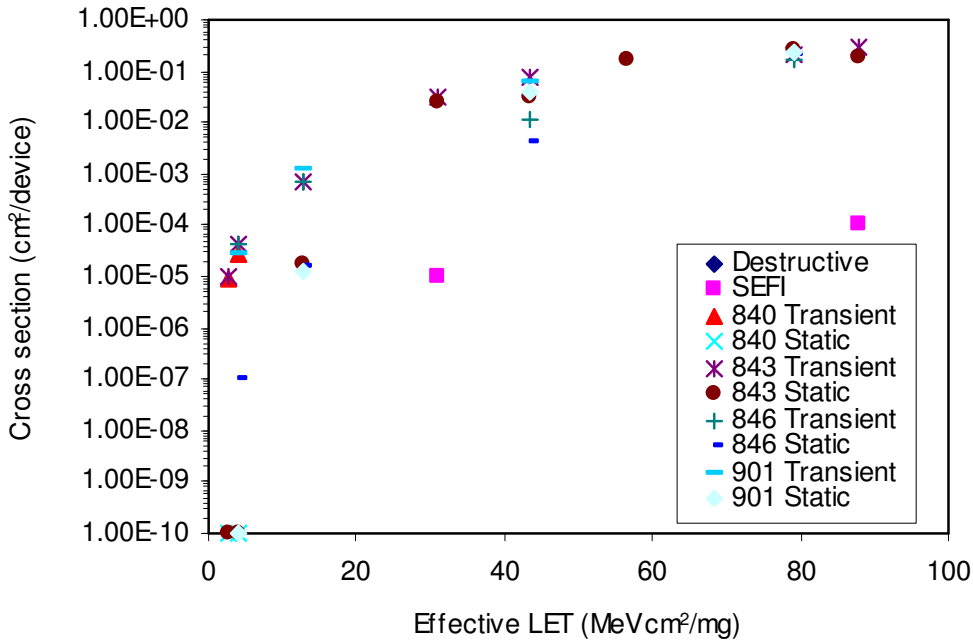

Fig. 6. Results for Dynamic Read mode.

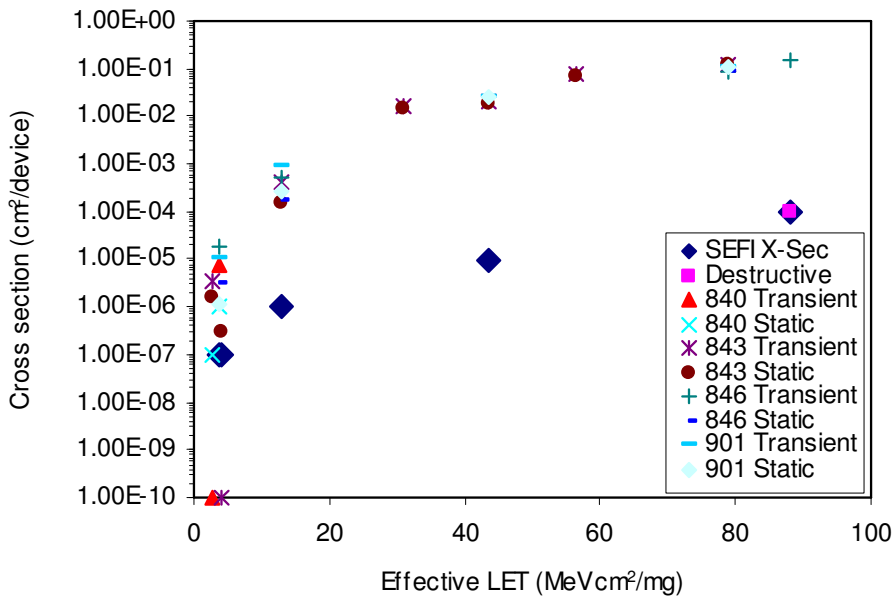

Fig. 7. Results in the dynamic R/W mode.

Results of the dynamic R/W tests are shown in Fig. 7. Generally these results are unremarkable, because the usual zero-to-one errors are rewritten as they occur. For this reason, there are fewer errors indicated than in Fig. 6, although the difference is not large. The main reason for including this test was the expectation that the high voltage write operation would contribute to more errors in the control circuits, which appears to have happened, but not on a large scale. Probably, this is because the write operation is performed only when a zero-to-one error is detected. For this circuit, there are relatively few such errors, so the write circuit duty cycle is a very small number. Where a static cross section is given, it is based on the number of errors detected after the exposure and resetting of the DUT, as before. The transient cross section is based on errors detected during the exposure. But some of the transient errors are probably really static bit errors that were rewritten during the test. In this mode, there were five SEFIs and one destructive event. The destructive failure was with Au ions at normal incidence (LDC 0846), when the erase operation could not be performed after the beam was turned off. This shot was also counted as a SEFI, because the DUT did not respond to commands until power was cycled. Two of the SEFIs were with Ne ions incident at 45 degrees (LDC 0840 and 0843). In both cases, the DUT would not respond to commands until power was cycled. There was one SEFI with Ar ions incident at 45 degrees (LDC 901). There were two page errors on that shot, which persisted after cycling power, but which were erased and rewritten successfully. There was also one SEFI with Kr ions at 45 degrees (LDC 0846), which was 65000 non-random errors. The DUT reset successfully.

Results for the room temperature dynamic R/E/W tests are shown in Fig 8. In this mode, errors are counted as they are read, but then they are erased and rewritten. Therefore, there are no static errors read after the beam is turned off, and bits in error for a time are counted as transient errors. Because the high voltage erase and program operations are performed constantly, it is expected there will be errors in the control logic in this mode. In fact, there were three SEFIs and two destructive failures in this mode, in addition to the high temperature results which will be discussed later. One SEFI and one destructive event occurred with Ar ions

incident at 45 degrees (LDC 0843). Immediately after the shot, the DUT did not respond to commands. After power was cycled, the part responded to commands, except that the write circuit had failed. With Au ions at normal incidence, there was also a SEFI with a destructive failure (LDC 901). This shot was counted as a SEFI because of multiple block errors, but the erase circuit also failed.

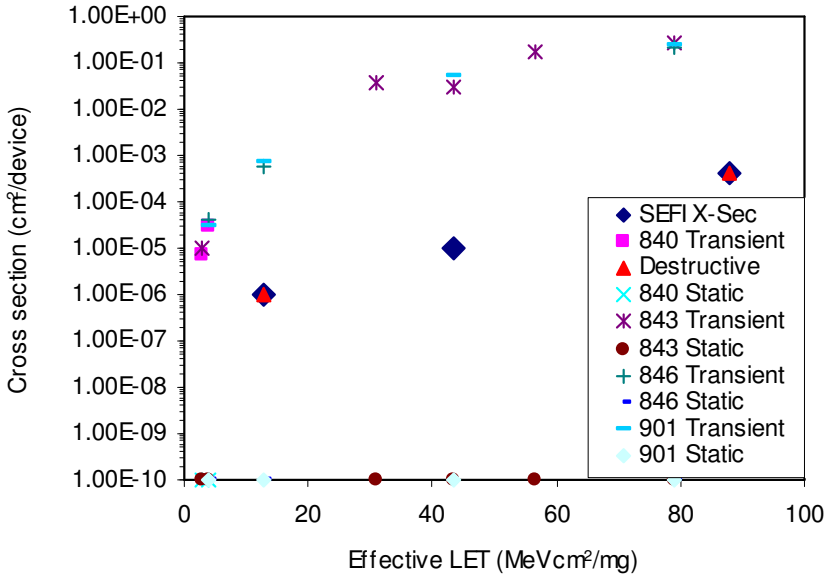

Fig. 8. Dynamic Read/Erase/Write results.

In addition to the room temperature results shown in Fig. 8, there were four shots at elevated temperature (70º C) and increased voltage (3.6 V) to test for SEL. All were using the R/E/W test mode, with Xe ions incident. In one shot, the ions were at normal incidence, and the DUT survived at a fluence of 10^5 particles/cm^2. A SEFI was recorded, but after power cycling, the DUT was successfully reprogrammed. In this case, the DUT was from LDC 901. In three other shots at 45 degree incidence, the DUTs all suffered write circuit failures at lower fluences (LDC 0901 and two parts from 0840). For every shot, the power supply current was monitored continuously, and it is clear from the current traces when these failures occurred. The current traces typically show a read current of about 10-11 mA, with pulses up to 15-16 mA when errors are being rewritten. When the write circuit starts to degrade, the write current will increase, but parts with current in the range of 22-23 mA have still functioned properly. On these shots, the current suddenly increased from 22-23 mA to 30 mA, then 40, then 50 mA, or more, which meant the part had failed. This high current was not the result of SEL, because current returned to normal when the DUT was told to stop writing—no power cycle was necessary. The DUTs all worked properly in read mode, and they could be erased, but not rewritten. Our best estimate of the fluence when failure occurred on these three parts is that the first two parts (LDC 901 and 840) both failed at about 25,000 particles/cm^2, and the third (LDC 840) failed at about 7,000 particles/cm^2. The reason there is some uncertainty in these numbers is that, although it is clear when the failure occurred, it is not clear from the current traces exactly when the beam was turned on. Additional analysis may clarify this point. In summary, there were three failures in about 57,000 incident particles at 45 degree incidence, or three failures in 157,000 total incident particles at high temperature. The flux at and above the LET of Xe in geosynchronous orbit is

about one particle/cm^2 per 125 years. If we take only the angular result as the worst case, that is approximately an average of 19,000 particles between failures, or about 2x10^5 chip-years between failures. To estimate the system failure rate, one would need to divide by N, the number of chips. In addition, the failures seem to occur in the high voltage write operation, which likely would not be performed constantly. For this reason, a duty cycle correction should probably be applied, which would tend to lower the failure rate. We note that many more shots were taken at room temperature, and similar failures were not observed, so there is a sensitivity at high temperature (and only at high temperature) that had not been noted before.

To estimate the error rate expected in space, given the cross sections in Figs. 4-8, we did one CRÈME96 run for geosynchronous orbit, using the following Weibull parameters: threshold LET=2.8, Width =37, exponent = 5, and saturation cross section = 7.5e-11 square microns. This curve bounds all five of the measured cross sections, with some margin in all cases. The result was a bit error rate of 6.35e-12, which is approximately five orders of magnitude better than a typical volatile memory. We note that the geosynchronous orbit is a more stringent environment than the planned MMS orbit, so the rate would be lower for the MMS orbit.

To estimate the impact of SEFIs, we can calculate that for geosynchronous orbit, the integral flux of particles at the LET of Ne and higher, is about 8500 particles/cm^2-year. In the entire run, there were 30 shots with Ne ions, for a total fluence of 3e8 particles/cm^2, which resulted in two SEFIs. That is, there were 1.5e8 particles per SEFI. Dividing by 8500 particles per year gives an estimate of 17,500 chip years between SEFIs. Similarly, for Ar ions, there were two SEFIs for 1.5e7 incident particles, for the entire run. The flux, in this case, is about 600 particles/cm^2-year, which leads to an estimate of one SEFI every 35,000 chip years. For Kr ions, there were five SEFIs from 1.6e6 incident particles, but the integral flux in space is only 0.36 particles per year. Therefore, one would estimate about 10^6 chip years between SEFIs. For Xe ions, there was one SEFI from 2.2e5 particles, and the flux is about one particle per 125 years. Therefore, the interval between SEFIs would be more than 2.5 million years. Most of these can be corrected by cycling power, and reprogramming the corrupted portion of the memory, so the impact to the mission should be manageable.

VII. Recommendations

The SEU response (single bit upset rate) of all NAND flash parts is excellent, compared with standard volatile memories, especially if error correction is used. The SEFI (Single Event Functional Interrupt) rate is of greater concern for space applications than the bit error rate, however. Typically, a SEFI occurs when a control circuit malfunctions as a result of a single ion interaction, and the entire memory, or a large part of it, fails. For standard volatile memories, this may mean reloading the entire memory from a backup, or even rebooting the entire system. The SEFI rate for these Samsung memories is relatively low, but recovery requires cycling power to the chip, and usually the affected portion of the memory has to be erased and rewritten. (For the Micron parts tested previously, it was often sufficient just to cycle power—no information was lost, in many of the SEFIs reported.) Here there are many fewer SEFIs, but information is lost in a higher percentage of them. Therefore, critical data would have to be backed up, to mitigate SEFIs.

VIII. Further Test Requirements

These Samsung parts have to be tested for total dose (TID) response, although previous testing suggests the response will be excellent. If these parts are going to be operated in space at elevated temperatures, we would recommend additional testing to determine the temperature dependence of the SEE response. At this point, we have data only at two temperatures. If the actual operating temperature is to be intermediate between those, it would certainly be logical to test at the actual operating temperature.

Static Unbiased Test Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
26	Ne/2.8	1.00E+06	0	0	N/A	0	
27	Ne/2.8	1.00E+07	0	0	N/A	0	
28	Ne/2.8	1.00E+07	0	0	N/A	0	
39	Ne/2.8	1.00E+06	0	0	N/A	0	
9	Ar/8.4	1.00E+04	0	0	N/A	0	
10	Ar/8.4	1.00E+06	0	0	N/A	1	
11	Ar/8.4	1.00E+07	0	0	N/A	26	
12	Ar/8.4	1.00E+07	0	0	N/A	22	
13	Ar/8.4	1.00E+07	0	1	N/A	3	45 degree incidence 3M bits
14	Ar/8.4	1.00E+07	1	0	N/A	3	45degree incidence--destructive failure
54	Kr	1.00E+04	0	0	N/A	13	
55	Kr	1.00E+04	0	0	N/A	10	
46	Xe	1.00E+06	0	1	N/A	8400	

Totals	Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
	Ne	2.20E+07	0	0	0	0	
	Ar	2.10E+07	49	0	5.80E-16	0	normal inc. only
	Kr	2.00E+04	23	0	2.90E-13	0	
	Xe	1.00E+06	8400	1	2.10E-12	1.00E-06	

Static Mode with Bias

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
29	Ne/2.8	1.00E+07	8	0	N/A	0	
30	Ne/2.8	1.00E+07	0	1	N/A	0	
40	Ne/2.8	1.00E+06	0	0	N/A	0	
41	Ne/2.8	1.00E+06	1	0	N/A	0	
1	Ar/8.4	1.00E+06	0	0	N/A	1	
2	Ar/8.4	1.00E+05	17	1	N/A	1	
3	Ar/8.4	1.00E+04	0	1	N/A	2	
4	Ar/8.4	1.00E+03	0	0	N/A	0	
5	Ar/8.4	1.00E+03	0	0	N/A	0	
6	Ar/8.4	1.00E+04	1	0	N/A	0	
7	Ar/8.4	1.00E+03	0	0	N/A	0	
8	Ar/8.4	1.00E+03	0	0	N/A	0	
56	Kr/29.3	1.00E+04	3	0	N/A	8	
57	Kr/29.3	1.00E+04	5	0	N/A	5	
47	Xe/53.9	1.00E+06	0	0	N/A	8657	
48	Xe/53.9	1.00E+06	1	1	N/A	appr. 4500	destr. Latch, no erase

Totals	Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
	Ne	2.20E+07	0	10	0	4.50E-07	
	Ar	1.12E+06	4	20	8.00E-16	1.77E-05	
	Kr	2.00E+04	13	8	2.90E-13	4.00E-04	
	Xe	2.00E+06	13150	2	2.18E-12	1.00E-06	

Dynamic Read Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
31	Ne/2.8	2.90E+06	8	1	??	0	
31	Ne/2.8	1.00E+06	1	1	??	0	
42	Ne/2.8	1.00E+06	3	0	18	0	
15	Ar/8.4	1.00E+04	1	0	3	0	
16	Ar/8.4	1.00E+03	0	0	0	0	
17	Ar/8.4	1.00E+03	0	0	0	1	
18	Ar/8.4	1.00E+04	1	0	0	1	
58	Kr/29.3	1.00E+04	4	0	40+	10	
59	Kr/29.3	1.00E+04	8	0	14	10	
52	Xe/53.9	1.00E+04	10	0	601	292	

Totals	Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
	Ne	4.90E+06	0	14	0	2.90E-06	
	Ar	2.20E+04	2	2	2.25E-14	9.10E-05	
	Kr	2.00E+04	20	12	2.50E-13	6.00E-04	
	Xe	1.00E+04	292	10	7.30E-12	1.00E-03	

Dynamic Read/Write Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
33	Ne/2.8	1.00E+06	1	0	??	0	
34	Ne/2.8	1.00E+06	0	0	??	0	
35	Ne/2.8	1.00E+06	0	1	??	0	
43	Ne/2.8	1.00E+06	1	0	??	0	
19	Ar/8.4	1.00E+04	5	0	??	1	
25	Ar/8.4	1.00E+04	1	0	??	3	
60	Kr/29.3	1.00E+04	5	0	17	2	
61	Kr/29.3	1.00E+04	10	0	14	4	
50	Xe/53.9	1.25E+04	14	0	117	28	
51	Xe/53.9	1.00E+04	11	0	188	10	

Totals	Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)
	Ne	4.00E+06	0	3	0	7.50E-07
	Ar	2.00E+04	4	6	5.00E-14	3.00E-04
	Kr	2.00E+04	6	15	7.50E-14	7.50E-04
	Xe	2.25E+04	38	25	4.23E-13	1.10E-03

Dynamic Read/Erase/Write Mode

Shot	Ion/LET	Fluence	Block Errors	Other SEFI	Transient Bit Errors	Static Bit Errors	Comments
36	Ne/2.8	1.00E+06	1	0	14	0	
37	Ne/2.8	1.00E+06	0	0	45	0	
38	Ne/2.8	1.00E+06	0	0	27	0	
44	Ne/2.8	1.00E+06	2	0	15	0	
45	Ne/2.8	1.00E+06	2	0	18	0	
20	Ar/8.4	1.00E+04	2	0	5	0	
21	Ar/8.4	1.00E+04	0	0	1	0	
22	Ar/8.4	1.00E+03	0	0	0	0	
23	Ar/8.4	1.00E+04	0	0	0	0	
24	Ar/8.4	1.00E+05	0	0	4	0	
62	Kr/29.3	1.00E+04	6	0	40	0	
63	Kr/29.3	1.00E+04	5	0	30	0	
64	Kr/29.3	1.00E+06	??	1	??	??	Every block affected--many errors
49	Xe/53.9	1.00E+06					Latchup--destructive, no erase
53	Xe/53.9	1.00E+04	15	0	77	3	

Totals	Ion	Fluence	Total bits	Total SEFI	Bit X-sec (cm2/bit)	SEFI X-sec (cm2/device)	Comments
	Ne	5.00E+06	0	5	0	1.00E-06	
	Ar	1.31E+05	0	2	0.00E+00	1.53E-05	
	Kr	1.02E+06	0	12	0.00E+00	5.50E-04	
	Xe	1.01E+06	3	15	7.50E-14	1.50E-03	