Guidelines for Design and Test of a Built-In Self Test (BIST) Circuit For Space Radiation Studies of High-Speed IC Technologies

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Presented by Marty Carts at the 2006 Single Event Effects Symposium, April 10, 2006 in Long Beach, CA.
The BIST Guidelines Document

- *This presentation introduces the detailed document by the same name.*

- *The BIST Guidelines document will be available on the Radiation Effects and Analysis Group’s website at NASA GSFC:*

  http://radhome.gsfc.nasa.gov
Outline

• Introduction
  – BIST
  – High speed single event testing
  – Sources of high speed single event test structures
• Aspects of a high speed BIST circuit
• CREST serial shift register
• SerDes Serializer/Deserializer
• Summary comments
Built-In Self Test (BIST)

- **Build some or all diagnostic circuitry into the device itself**
- **BIST exists all over:**
  - Parametric Analyzers
  - Handheld DMM (Auto-zeroing)
  - Computers, (RAM testing on Boot)
  - Radio Stations (Broadcast Test Signal to Monitoring Stations)
  - Integrated Circuits (SerDes)
- **BIST hasn’t been implemented in many single event test applications (yet)**

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High Speed Single Event Testing

- Single event susceptibility tends to rise with increasing frequency
- Hardening techniques complicate susceptibility vs frequency behavior
- The nature of error events changes with frequency
- Bit Error Rate Test (BERT) Equipment
  - Generator, Analyzer

![Diagram of BERT testing process]

- Geometric Bandwidth effectively decreases with increasing $F_{max}$
- Cost Rises quickly with increasing $F_{max}$
Sources of High Speed Single Event Test Devices

- **Specific Integrated Circuits**
  - Requires significant external equipment, including BERT
  - Not optimized for results generation

- E.g. AD8151 fabric switch (see Buchner, et.al 2003 RADECS)
Sources of High Speed Single Event Test Devices

- **IC fabrication test structures**
  - Single transistors, capacitors, inverters, flipflops, shift registers
  - May not be optimized for high speed operation
  - May not optimized for large area data collection
  - Still require equipment of equal or better speed

- **High speed BIST test structures**
  - Allow testing independent of BERT equipment
  - Designed to run at device’s Fmax, even beyond available test equipment
  - Designed to gather the right data
  - Available early in the process lifetime
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Aspects of H.S. BIST Device

- Test Structure
  - Primary target for single events
  - Type per requirements (science data or application specified)
  - Test Structure Types
    - Shift register
    - SerDes
    - Buffers
    - PLL
    - Others?
Aspects of H.S. BIST Device

- **Error Detection and Data**
  - Choice closely coupled to Test Structure
  - As simple as possible
    - Complexity will tend to cloud results
    - Allows maximization of test structure area
    - Increases probability of 1st pass design success
  - Example:
    - Test Structure
      - Shift Register (with its clock tree)
      - 127 bits long
    - Error Detection
      - XOR Difference Detector at bit 0 and bit 127
    - Data
      - PN7 \( (2^7-1) \text{ PRBS} \)
      - (Any repeating 127 bit pattern would do)
Aspects of H.S. BIST Device

- Test structure, error detection, data highly coupled. Example:
  - Test Structure = 127 bit Shift Register (w/clock tree)
  - Error Detection = XOR gate
  - Data = PN7 (2^7-1 PRBS but any repeating 127 bit pattern would do)
Aspects of H.S. BIST Device

• Results Selection
  – Assure access to the required data
  – Opportunity (and last chance!) to optimize data gathered for test goals
  – Treat encoding/decoding carefully
Aspects of H.S. BIST Device

- Results Storage
  - It’s impractical to save *all* data
  - Upon an error event, the Results Set must be stored until it can be collected
  - Shift register (CREST) example:
    - Must accommodate delay in clock-stop circuit
    - (Results Selection: Collect E Data too!)

![Diagram of the test structure with 127-bit long shift register and data-saving FIFO]
Aspects of H.S. BIST Device

• Self-Contained High Speed Circuitry
  – It is a PAIN to handle high speed signals
    • Loss/phase dispersion cabling issue
    • Signal timing issue
    • Signal conditioning issue
  – Generate data on-die if possible
  – Generate clock on-die if possible!
  – Allow “low” speed data outloading
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Serial Shift Register Example

- CREST was actually designed, built and tested. See:

  “Autonomous Bit Error Rate Testing at Multi-Gbit/s Rates Implemented in a 5AM SiGe Circuit for Radiation Effects Self Test (CREST),”

P. Marshall, et. al

Serial Shift Register Example

The Test Structure (127 bit long shift register)

Data-saving FIFO

The Error Detection and Latch Circuitry

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Serial Shift Register Example

CREST Clock Control Circuit
CREST Die Wirebonded to PCB
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Serializer/Deserializer Example

- Serial link is economical
- Serializes N bit wide parallel system data
- Serial output rate >= N times parallel rate
- Deserializer restacks data into parallel form
- Two PLLs involved
- BIST frequently already included...
Serializer/Deserializer Example

- BIST additions shown in red
- 2 options for high speed BIST:
  - Loop back in parallel path
  - Loop back in serial path
- Parallel loop back allows for correlation to BERT testing
- Serial loop back allows lower speed testing
Serializer/Deserializer Example

- **SerDes Issues:**
  - PLL hits--Loong stretches of garbled data.
  - Encoder/Decoder hits--Garbled data
  - Encoder hits--Deserializer lock loss
  - Decoder hits--Word Sync Reacquisition time

- **BIST Aspects**
  - Test structure/Data/Error detector
  - Results/Results Storage

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• SerDes Issues
  – Complexity--Many diverse functions
  – PLLs will have different error signatures in addition to other circuitry
  – Possible total event data loss due to complexity
  – Latency due to PLL settings
  – Word latency due to Serializer, Deserializer, possible parallel input FIFO
  – Test structure/Data/Error detector
  – Results/Results Storage
Summary

• BIST for high speed single event test is the best approach for
  – Wide bandwidth testing (above ~12 GBPS)
  – Testing in absence of expensive equipment

• BIST approach allows for test optimization
  – Die area devoted to data collection
  – Test Results.

• BIST approach has been proven in 5AM SiGe and the
• Lessons learned and extrapolated wisdom are summarized in NASA document,

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