Radiation Testing Considerations for Advanced CMOS Electronics

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Thank You to Sponsors and Collaborators

• Sponsors
  – NASA Electronic Parts and Packaging (NEPP) program
  – Defense Threat Reduction Agency (DTRA)

• Collaborators
  – NASA/GSFC Radiation Effects and Analysis Group (REAG)
  – IBM Corp.
    • Ken Rodbell et al.
  – Intel Corp.
    • Balkaran Gill, Norbert Seifert, et al.
  – Jazz Semiconductor
    • Scott Jordan, et al.
  – Naval Research Laboratory
    • Steve Buchner, Hap Hughes, Dale McMorrow, et al.
  – Sandia National Laboratories
    • Paul Dodd, Marty Shaneyfelt, Jim Schwank, et al.
  – Texas Instruments
    • Rob Baumann, Xiaowei Deng, Andrew Marshall, et al.
  – Vanderbilt University
    • Nathaniel Dodds, Lloyd Massengill, Robert Reed, Ron Schrimpf, Robert Weller, et al.
**Goal Statement**

For advanced CMOS electronics:

Gather necessary data to ensure that you can accurately bound the risk for a given mission application

- Two risks
  - Decide to fly the part “as is” when the risk of failure is unacceptably high
  - Decide part requires remediation (i.e., testing) when its failure probability was sufficiently small “as is”


CMOS = complimentary metal oxide semiconductor

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**Outline**

- Describe two flavors of advanced CMOS
  - Commercial-off-the-shelf (COTS)
  - Radiation-tolerant standard products and application specific integrated circuits (ASICs)
- Define “necessary data”
  - Total ionizing dose
  - Single-event effects <-> key driver
- Question how we “accurately bound the risk” for a given mission
  - Phenomenological,
  - Analytical, and
  - Statistical techniques
- Conclusions
Advanced CMOS Flavors

• COTS
  – Designed with no attempt to mitigate radiation effects. COTS can refer to commodity devices or to ASICs designed using a commercially available design system.

• Radiation-tolerant
  – Designed explicitly to account for and mitigate radiation effects.
    • By process and/or design

Examples of Advanced CMOS

• COTS
  – Synchronous dynamic random-access memory (SDRAM)
  – Flash memory and other non-volatile solutions
  – Data converters
  – High-speed amplifiers
  – Digital signal and multi-core processors
  – Field programmable gate arrays (FPGAs)

• Radiation-Tolerant
  – RHBD + RHBP in boutique foundries
  – RHBD applied to AMS, IBM, Jazz, ONsemi, or TSMC ≤ 90 nm bulk/SOI CMOS
  – Use of pre-processed (i.e., hardened) silicon substrates in commercial process flows
  – FPGAs

AMS = AustriaMicroSystems
TSMC = Taiwan Semiconductor Manufacturing Co.; SOI = silicon-on-insulator
RHBD = radiation-hardened by design; RHBP = radiation-hardened by process
Total Ionizing Dose (TID) Data

• One bright spot for most missions that use highly-scaled technologies
• Thinner oxides have led to increased TID tolerance
  – For NASA, meets most mission requirements
• One exception might be N. F. Haddad et al., IEEE TNS, 2009.
  High-perform W/L = 5/0.08 SDRAM at a rate floating gate (FG) non-volatile memories
  – FG cells and charge pump are susceptible to TID


Total Ionizing Dose (TID) Data

Analog Devices AD5544 CMOS 16-bit Digital-to-Analog Converter
(0.5 μm CMOS used to demonstrate a point)

• Part-to-part and lot-to-lot variability
  – Affects number of components that must be tested to bound risk
  – Limits usefulness of heritage data
  – Tied to bias conditions and temperature – combined effects

Thank you to the NASA Magnetospheric MultiScale (MMS) Mission for testing support

To be published on http://nepp.nasa.gov/.
**Bounding TID Risk**

- Test more hardware – easiest answer
  - Example: 22 trials (i.e., parts) with 0 failures establishes $p_s > 90\%$ with 90\% confidence (binomial distribution)
  - Not always possible due to schedule, budget, hardware availability

- Define part-to-part and lot-to-lot variability – dictates how many components should be tested
  - Consideration for development phase with a process
  - Use kerf structures to gather test data on multiple wafer lots
  - Perhaps easier with qualified processes

- Utilize heritage (suspension) and similarity data, if available, to augment analysis

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**Single-Event Effect (SEE) Data**

- Destructive SEE can still be an issue with advanced bulk CMOS
  - Dependent on
    - Rail voltage
    - Layout constraints
    - Temperature (cryogenic latchup)

- Solutions include
  - Efficient well contacting
  - Hardened silicon wafers or SOI process

SRAM = static random access memory
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Contours are boundary where $V_{\text{hold}} = V_{dd}$
- Below = vulnerable; above = immune
- A-C = anode-cathode spacing

Sample SDRAM SEE Test Data

- Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects
  - Small event counts for effects like functional interrupts – often depend on state, location, etc.

K. A. LaBel et al., IEEE TNS, 2008.
Single-Event Effect (SEE) Data

45 nm SOI CMOS SRAM

90 nm bulk CMOS SRAM cell varieties

• Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects
  – Potential threats from low-energy protons

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Single-Event Effect (SEE) Data

32 nm SOI CMOS latch cross sections – contours are based on data & simulation

• Non-destructive SEE continue to be the most difficult aspect of advanced CMOS radiation effects
  – Varied angular sensitivity (test considerations)

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Bounding SEE Risk

- Investigate risk of destructive events like latchup in bulk CMOS
- Recognize importance of roll and tilt angle sensitivities
  - Large-angle irradiations are critical
  - Test setup and packaging considerations
  - Observed in both SRAM and latches
- Choose the right tool to interpret the data and get an on-orbit event rate
  - From Figure of Merit to full, multi-dimensional Monte Carlo

Summary

- Size, weight, and power benefits of advanced CMOS dictate its use in certain applications
- TID performance is acceptable as-is in many cases
- SEEes are real radiation driver concerning advanced CMOS
  - Risk of destructive effects still exists in bulk CMOS,
  - Rare non-destructive effects like functional interrupts,
  - Low-energy proton sensitivity, and
  - Angular effects that place requirements on test setup, packaging, and ion beam characteristics
- Real need for simulation tools capable of both informing data collection and extrapolating data sets to yield on-orbit rates
  - See, for example, R. A. Weller et al., IEEE TNS, 2010.