Samsung 16G NAND Flash Memory SEE Test Report

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Test Date: May 18, 2012  Report Date: June 21, 2012

I. Introduction

This study was undertaken to determine and compare the susceptibilities of 16 Gbit NAND Flash memories from Samsung (part number K9FAG08U0M) to destructive and nondestructive single-event effects (SEE) for use in possible future NASA missions. The devices were monitored for SEUs, errors from individual cells, for SEFIs, errors arising in the control logic, and for destructive events, including latchup, induced by exposing them to a heavy ion beam at the LBNL (Lawrence Berkeley National Laboratory) Cyclotron.

II. Devices Tested

In this test, two parts were used (part number K9FAG08U0M-HCB0, Lot Date Code (LDC) 1043). The parts have 2Gx8 organization with large blocks. That is, the blocks are (512K+40K)x8, with 64 pages/block. Each page is nominally 8Kx8, but they also have 640 redundant columns, which makes the total page size (8K+640)x8. NAND flash normally has some bad blocks which can be screened off. The specification is that 4056 of the 4152 blocks will be good. In our experience, the parts almost always have a few bad blocks, but it is usually a single digit number. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility.

The device technology is 32 nm minimum feature size CMOS NAND Flash memory. All the parts are single die, SLC (single level cells). The chips came in a 132-pin BGA package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface.

III. Test Facilities

Facility: LBNL Cyclotron
Flux: \((5 \times 10^3 \text{ to } 1. \times 10^5 \text{ particles/cm}^2/\text{s})\).
Fluence: All tests were run to 1E3 to 1E8 ions/cm\(^2\), or until destructive or functional events occurred.
IV. Test Conditions

Test Temperature: Room Temperature.
Operating Frequency: (0-40 MHz).
Power Supply Voltage: 3.3V. Standard test methods for SEU testing (e.g., ASTM 1192) call for testing at nominal voltage less 10%, because SEU in standard volatile memories is caused by voltages being pulled down. However we are also looking for control logic errors, which are thought to be due to things turning on when they are not supposed to be on. Reduced voltage would, therefore, cause an underestimate of the rate for these events. For this reason, we used nominal voltage, 3.3 V, in all tests.

V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Test patterns included all 0’s, all 1’s, checkerboard and inverse checkerboard. In general, all zeroes is the worst-case condition for single bit errors. For a zero, the floating gate is fully charged with electrons. An ion can have the effect of introducing positive charge, which may be enough to cause a zero-to-one error. However, a checkerboard pattern (AA) was used in many tests because errors in the control circuitry can cause errors of both polarities. One-to-zero errors are an indication that the errors are coming from the control circuits. Between exposures, all patterns can used to exercise the DUT, to verify that it was still fully functional. However, all patterns are not used routinely, just because it is too time consuming to do so. The maximum clock frequency for these devices was 40 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.
Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation. It was also not possible to monitor the power supply current during the unbiased tests, but this was done in all the other test modes.

3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation, and the errors counted. This condition allows determination of functional, configuration and hard errors, as well as bit errors. In this mode, the number of static bit errors is determined by reading the memory again, after the beam is turned off. In reporting for this test mode, we normally distinguish between transient errors, due to transient noise in the Read circuit, and static errors, where the bits are actually corrupted.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a word in error was rewritten. In this mode, the words that are read are compared to the stored pattern. When errors are detected, the addresses are rewritten. Because the Write operation uses the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions in this test mode. In this mode, a block is Read, and rewritten, if necessary, followed by the next block, and so on. Note that this mode only corrects one polarity of error, which is zero-to-one.

5) Dynamic Read/Erase/Write, which is similar to the R/W mode, except that it corrects both polarities of errors. A block in error is Erased, and then rewritten. Since the high voltage charge pump is used for both the Erase and Write operations, it is expected that the parts will be most vulnerable to destructive effects in this mode.

6) In this set of experiments, we have attempted to look at angular effects, which may include multiple bits grazed by the same ion, and other effects due to charge sharing by multiple nodes in the control logic. This test was done with the DUT tilted 45 degrees. In previous testing, with TSOP packaged parts, the socket used to hold the DUT prevented tests at any higher angle. This restriction does not really apply with the BGA package, but there was not enough beam time to test at a variety of angles. Since we only had time for one angle, we used the same angle we had used previously, which allows us to compare these results with previous tests.

The Block diagram for control of the DUT is shown in Figure 2. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the flash is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for over-current conditions and shuts down power to the DUT if such conditions are detected.
Figure 2. Overall Block Diagram for the testing of the NAND Flash.

(a) Front
VI. Results

During testing, the DUTs were irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam, or at 45 degrees. The errors observed in static SEU testing are shown in Fig. 4, with no bias applied. The 45 degree data is plotted at the effective LET (LET/cos θ). This is done so that one can distinguish between the normal incidence shots and the 45 degree shots. It is not done because effective LET is expected to be a useful concept for other reasons. In Fig. 4, the cross section for bit errors is plotted in units of cm²/bit. In this mode, there were no SEFIs of functional failures (destructive effects). The same results are plotted in Fig. 5, in units of cm²/device, which we normally do so that SEFIs and functional failures can be plotted on the same scale as bit errors. In this case, there are not any such events, so there is no real difference between the plots. In Fig. 4, the red squares indicate a Weibull curve fitted to the measured cross section, where the threshold LET is taken to be 1 MeV/mg/cm², the width, W, is taken to be 15 MeV/mg/cm², the exponent or shape factor is 5.0, and the saturated cross section is taken to be 3x10⁻¹¹ cm². These parameters were used to calculate the Petersen Figure of Merit (FOM) [1-3], which was used, in turn, to estimate the bit error rate for the Adams worst case environment (geosynchronous orbit at solar minimum). In this case, the FOM is approximately 1.86 x 10⁻¹¹, which corresponds to an error rate of about 5 x 10⁻¹¹ errors/bit-day. This is slightly higher than previous generations of Samsung NAND flash technology [4], but not unexpected, however.
Fig. 4. Blue diamonds indicate single bit error cross section in static unbiased mode, for the Samsung 16G NAND flash memory. Red squares indicate Weibull curve fitted to data and used in the error rate calculation.
Fig. 5. Bit error cross section, along with cross sections for SEFIs and functional failures, shown on the same scale for static unbiased mode, for the Samsung 16G NAND flash memory. Points plotted at $10^{-10}$ cm$^2$ (pink squares and red triangles for SEFIs and functional failures) are really zeroes.

Fig. 6. SEU, SEFI, and Destructive results for static mode, with bias applied.

The results for static mode with bias applied are shown in Fig. 6. The main effect is single bit upsets (blue diamonds), along with no SEFIs (pink squares), and no destructive events (yellow triangles), again. The bit error rate is essentially the same as for the unbiased condition, as shown in Fig. 5.

Fig. 7. Results for the Samsung 16G NAND flash in Dynamic Read mode. Transient (teal X) and static errors (red triangles) are shown, along with one SEFI (purple symbol), from Kr ions at 45° incidence. There were no functional failures (brown circles).
For the Dynamic Read condition, the parts showed exhibited transient read errors in addition to the bit errors, which are plotted in Fig. 7. In this mode, the DUT reads continuously with the beam on. The significance of the transient errors is not always completely clear, because the entire memory can be read multiple times, which means static errors will be read multiple times. On the other hand, sometimes the beam is turned off before even one loop through the memory is completed, in which case some static errors will not be counted at all, until after the beam is off. In addition there are errors due to transient noise in the read circuit or the control logic. The static errors shown in Fig 7 are bit errors read after the beam is turned off. Generally the static error count and the transient error count are similar, which suggests that the transient errors are really just static bit errors. For the one shot with a SEFI, it was not possible to determine the static error count. The reason was that there were so many control logic errors that they swamped the handful of real bit errors.

Results of the dynamic R/W tests are shown in Fig. 8. The main reason for including this test was the expectation that the high voltage write operation would contribute to more errors in the control circuits, which does not appear to have happened. There were no functional failures, and only one SEFI, which was, again, with Kr at 45° incidence. The only puzzling result here is that the static errors and transient errors appear to be roughly equal. The problem is that the static errors are supposed to be corrected in this mode. Probably, we did not wait long enough after the beam was off to stop the rewrite operation, which prevented some of the errors from being corrected.

Results for the dynamic R/E/W tests are shown in Fig 9. In this mode, errors are counted as they are read, but then they are erased and rewritten. Therefore, there are no static errors read after the beam is turned off, and bits in error for a time are counted as transient errors. Because the high voltage erase and program operations are performed constantly, it is expected there will be errors in the control logic in this mode. In fact, there were multiple SEFIs and one destructive failure in this mode. The point indicating a SEFI at LET ~30 MeV·cm²/mg is actually three points, superimposed. The failure was with Kr ions at 45° incidence. After the first part failed, a second part was used for another shot with Kr, and for all the shots with Xe. There were SEFIs on both Xe shots in this mode, but no functional failure, even though Xe might be expected to be more damaging than Kr. On the shots where there were SEFIs, it was not possible to count the single bit errors because there were so many control logic errors. There was no Xe shot at normal incidence because we ran out of time, but there was a Xe shot at high angle.
Fig. 9. SEU, SEFI, and Destructive results in Dynamic Read/Erase/Write mode. In this mode errors are corrected as they occur (indicated by pink squares), except that the number cannot be determined when SEFIs (purple symbols) or functional failures (brown circles) occur.

Samsung 16G NAND
Fig. 10. Write current as a function of number of exposures, indicating the buildup of cumulative damage over many shots.

In Fig. 10, we illustrate a pattern we have observed numerous times. In this case, a fresh part has write current of 18.5 mA, but as the part is exposed to one beam run after another, the write current increases to 20 mA to 22 mA to 25 mA, and then the part fails, as it does here. After failure, the write current jumps up to 30 mA, in this case. In a case like this, we report the failure by plotting it for the shot where it was observed, as in Fig. 9, here. But the failure is clearly the result of cumulative damage, and not something that happened on just the last shot. In this case, the failure occurred on a shot with Kr ions at high angle, but a fresh part survived a similar, later, shot with Xe ions. One would expect the shot with Xe to be a more severe test, because of the higher LET. We have to report failures if they occur, and if we did not plot them where they occurred, where would we plot them? But it is important to recognize that they are not usually due to single ion interactions, but rather to cumulative damage from many shots.

We also note that in the Dynamic R/W mode, every shot with Kr ions produced a SEFI, which all happened just before the part failed. In the same test mode, a fresh part exposed to Xe ions had no SEFIs, even though Xe has a higher LET, and so would be expected to be more disruptive. Although this one example is not conclusive, it suggests that some of the SEFIs we observe might be the result of cumulative damage, also. If it is eventually confirmed that parts with accumulated damage are more sensitive to SEFIs, it should not be surprising.

Conclusions

The Samsung 16G NAND flash appears to be reasonably robust against heavy ion-induced single event effects (SEE). The bit error rate estimated in the discussion of Fig. 4, $5 \times 10^{-11}$ errors/bit-day is orders of magnitude better than most standard volatile memories. As we have pointed out, this is a slightly higher error rate than estimated for previous technology generations of Samsung NAND flash, which is generally expected because the number of electrons representing the difference between a zero and a one is smaller in each succeeding technology generation. Therefore, less charge has to be deposited to cause an error. On the other hand, the geometrical cross section is also smaller, meaning that each bit has a smaller probability of being hit by an ion, which largely offsets the effect of smaller critical charge. The result is that the difference from one technology generation to the next is small, but not zero. We note that $5 \times 10^{-11}$ errors/bit-day in a 16G chip is equivalent to 0.8 chip errors/day. The Samsung 16G NAND has redundant memory built in sufficient to install SEC/DED (single error correction/double error detection) Hamming code capable of correcting one bit of every 512 bits. This means that up to N = 32M single errors could be corrected, if they were properly spaced. For randomly distributed errors, the probability of an uncorrectable double error is about 50% after $(N\pi/2)^{1/2}$ single errors, or a little more than 7000 errors, which would accumulate in about 8900 days, if the memory were never scrubbed or refreshed. This is almost 25 years in geosynchronous orbit—the interval would be longer in most other orbits. To our knowledge, the only NASA mission to operate longer than this is one of the Voyager spacecraft, launched in the late 1970s. But if the Voyager had stopped working after 25 years, no one would have complained.

The SEFI cross section is about $10^{-5}$ cm$^2$ with Kr ions, and about $10^{-4}$ cm$^2$ for Xe. In geosynchronous orbit, the flux at the LET of Kr is about one ion/cm$^2$ every 18 years, and about one ion/cm$^2$ every 125 years for Xe, according to the CREME96 input spectrum [5]. As we have indicated in the discussion above, cumulative damage over many shots may have contributed to some of these. The event rate is unlikely to be more than one event per $10^6$ chip-years in orbit, regardless. The only functional failure
was clearly due to damage accumulated over many beam runs, corresponding to millions, or perhaps even billions of years in orbit.

Even so, the Samsung 16G NAND cannot be recommended until it is also tested for TID (total ionizing dose). However, previous generations of Samsung NAND technology have had excellent TID response.

References