Test Report:
Total Dose Test of the 54AC273 Octal Flip-Flop Manufactured by National Semiconductor

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I. Introduction

The radiation sensitivity of the clock threshold voltages for latching data, i.e., from low to high ($V_{th}(L)$) and from high to low ($V_{th}(H)$) were determined for the 54AC273 flip-flop by measuring the values before and after exposure to a Total Ionizing Dose (TID) of 10 krad(Si). Two parts were exposed to radiation and another two parts were kept as controls. $V_{th}(L)$ and $V_{th}(H)$ were measured for all four parts prior to and following irradiation so that any changes in the irradiated parts could be determined. The test showed that both $V_{th}(H)$ and $V_{th}(L)$ changed by at most 20 mV after a TID of 10 krad(Si), a value that is well within the specifications for the subsystem.

II. Background

The 54AC273 is an octal D-type flip-flop used to switch the Solid State Power Controller (SSPC) on all the Low Power Switch Cards (LPSC) on Solar Dynamics Observatory. The signals controlling the 54AC273 are provided by an FPGA (Actel) which is a 3.3 V part. Because the minimum threshold voltage for the clock to latch the data is given in the data sheet as 3.5 V when the supply is 5 V, a level shifter was inserted between the FPGA and the 54AC273 to provide sufficient margin to ensure that the data are properly latched into the flip-flop. All data inputs to the 54AC273 were routed through the level-shifter, except for the clock signal, which was inadvertently connected directly between the FPGA and the 54AC273. [The D-type flip-flop on the ETU board was a 54ACTQ273 which has a lower clock threshold voltage for latching the data (2.0 V) and was, therefore, compatible with the 3.5 V output of the FPGA.]

Testing, under a variety of conditions, of the LPSC board indicated that the 54AC273 operated properly in spite of the clock signal from the FPGA having a maximum voltage of 3.3 V, i.e., data could be latched into the flip-flops at a clock edge. The question this test was designed to answer was whether, following a total dose of 10 krad (Si), the threshold voltages for the clock had degraded to the point that the data could no longer be latched into the 54AC273 flip-flop.

III. Part Information

Table I contains information on the part and test conditions. Fig. 1 shows the pin-out for the device.

Table I
Information on Part and Test Conditions

Project:	SDO
Subsystem:	Low Power Switch Card
Part Type:	Microcircuit, Digital, ACMOS, Flip-flop
Manufacturer :	National Semiconductor
Part Number :	M38510R75601S2A
Generic Part Number :	54AC273
Date Code :	0502A
Lot Quantity :	4 (2 irradiated and 2 controls)
Total Dose :	10 krad(Si)
Dose Rate :	10 rads(Si)/s

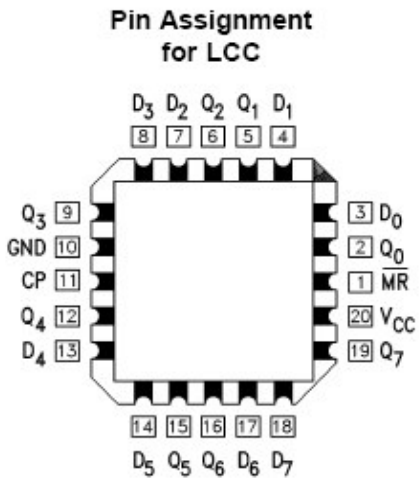

Fig. 1. Pin-out for the 20-pin LCC package of the 54AC273.

IV. Test Procedure

Prior to irradiation all four parts were electrically tested by measuring the threshold voltage for latching both high and low values. The procedure consisted of the following steps:

- Test for VIH_MIN
  Set D equal to 2.0 V and decrease the clock voltage from 3.0 V in steps of 10 mV until device fails.
- Test for VIL_MAX:
  Set D equal to 3.0 V and increase the clock voltage from 2.0 V in steps of 10 mV until device fails.

The test was carried out for all eight flip-flops in each device. The test was repeated for three supply voltages (5.5 V, 5.0 V and 4.5 V) and three temperatures (Room temperature, +80 C and -20 C).

Two parts were inserted in 20-pin LCC sockets attached to a board which was placed in a box consisting of layers of aluminum and lead in front of a Co^{60} source. During irradiation, the parts were maintained at room temperature. A power supply provided 5 V to V_{dd}. All the inputs were grounded and the outputs were left floating. The parts were irradiated to a total dose of 10 krad(Si) at a dose rate of 10 rads(Si)/s. After irradiation, all four parts were re-tested electrically to ascertain whether any changes occurred in the clock threshold voltages.

V. Results.

The results of the test are shown below. Devices 145 and 142 were irradiated, whereas devices 144 and 143 were not irradiated. The data show small shifts in the threshold voltages following irradiation, with maximum shifts of 30 mV. In general the small radiation induced shifts resulted in a lowering of the VIL and VIH improving margin with respect to the 3.3 V Actel FPGA driving the clock.

Device 145			0 krad	0 krad	10 krad	10 krad
Vcc (V)	Temp.(C)	Channel	VIH_MIN	VIL_MAX	VIH_MIN	VIL_MAX
5.5	22	Q0	2.74	2.77	2.72	2.75
5.5	22	Q1	2.74	2.77	2.72	2.75
5.5	22	Q2	2.74	2.77	2.72	2.75
5.5	22	Q3	2.74	2.78	2.72	2.75
5.5	22	Q4	2.74	2.78	2.72	2.76
5.5	22	Q5	2.74	2.78	2.72	2.75
5.5	22	Q6	2.74	2.78	2.72	2.76
5.5	22	Q7	2.69	2.80	2.68	2.78
5.0	22	Q0	2.52	2.54	2.51	2.52
5.0	22	Q1	2.52	2.53	2.51	2.52
5.0	22	Q2	2.52	2.54	2.51	2.52
5.0	22	Q3	2.52	2.54	2.51	2.51
5.0	22	Q4	2.52	2.54	2.51	2.51
5.0	22	Q5	2.52	2.54	2.51	2.52
5.0	22	Q6	2.52	2.54	2.51	2.52
5.0	22	Q7	2.49	2.58	2.48	2.55
4.5	22	Q0	2.31	2.31	2.30	2.29
4.5	22	Q1	2.31	2.30	2.29	2.28
4.5	22	Q2	2.31	2.30	2.29	2.28
4.5	22	Q3	2.31	2.30	2.30	2.28
4.5	22	Q4	2.31	2.31	2.30	2.29
4.5	22	Q5	2.31	2.31	2.29	2.29
4.5	22	Q6	2.31	2.31	2.30	2.28
4.5	22	Q7	2.31	2.37	2.29	2.33

Device 142			0 krad	0 krad	10 krad	10 krad
Vcc (V)	Temp.(C)	Channel	VIH_MIN	VIL_MAX	VIH_MIN	VIL_MAX
5.5	22	Q0	2.73	2.78	2.72	2.76
5.5	22	Q1	2.73	2.78	2.72	2.75
5.5	22	Q2	2.73	2.78	2.72	2.75
5.5	22	Q3	2.73	2.75	2.72	2.76
5.5	22	Q4	2.74	2.79	2.72	2.76
5.5	22	Q5	2.73	2.78	2.72	2.76
5.5	22	Q6	2.73	2.78	2.72	2.76
5.5	22	Q7	2.68	2.80	2.67	2.78
5.0	22	Q0	2.52	2.54	2.51	2.52
5.0	22	Q1	2.52	2.54	2.51	2.52
5.0	22	Q2	2.52	2.54	2.51	2.52
5.0	22	Q3	2.52	2.54	2.50	2.52
5.0	22	Q4	2.52	2.54	2.51	2.53
5.0	22	Q5	2.52	2.55	2.51	2.52
5.0	22	Q6	2.52	2.55	2.51	2.52
5.0	22	Q7	2.48	2.58	2.47	2.55
4.5	22	Q0	2.31	2.31	2.29	2.29
4.5	22	Q1	2.31	2.31	2.29	2.29
4.5	22	Q2	2.30	2.31	2.29	2.28
4.5	22	Q3	2.31	2.31	2.29	2.29
4.5	22	Q4	2.31	2.31	2.29	2.29
4.5	22	Q5	2.31	2.31	2.29	2.29
4.5	22	Q6	2.31	2.31	2.29	2.29
4.5	22	Q7	2.30	2.35	2.29	2.34

Device 144			0 krad	0 krad	0 krad	0 krad
Vcc (V)	Temp.(C)	Channel	VIH_MIN	VIL_MAX	VIH_MIN	VIL_MAX
5.5	22	Q0	2.72	2.76	2.72	2.79
5.5	22	Q1	2.72	2.75	2.72	2.78
5.5	22	Q2	2.72	2.75	2.72	2.78
5.5	22	Q3	2.72	2.75	2.72	2.78
5.5	22	Q4	2.72	2.76	2.72	2.78
5.5	22	Q5	2.72	2.76	2.72	2.79
5.5	22	Q6	2.72	2.77	2.72	2.78
5.5	22	Q7	2.68	2.76	2.67	2.80
5.0	22	Q0	2.51	2.53	2.51	2.55
5.0	22	Q1	2.51	2.53	2.51	2.54
5.0	22	Q2	2.51	2.53	2.51	2.54
5.0	22	Q3	2.51	2.53	2.51	2.54
5.0	22	Q4	2.51	2.53	2.51	2.54
5.0	22	Q5	2.51	2.53	2.51	2.55
5.0	22	Q6	2.51	2.53	2.51	2.54
5.0	22	Q7	2.48	2.53	2.47	2.57
4.5	22	Q0	2.30	2.30	2.30	2.31
4.5	22	Q1	2.30	2.31	2.30	2.31
4.5	22	Q2	2.30	2.31	2.30	2.31
4.5	22	Q3	2.30	2.30	2.30	2.31
4.5	22	Q4	2.30	2.31	2.30	2.31
4.5	22	Q5	2.30	2.31	2.30	2.31
4.5	22	Q6	2.30	2.31	2.30	2.31
4.5	22	Q7	2.29	2.31	2.30	2.36

Device 143			0 krad	0 krad	0 krad	0 krad
Vcc (V)	Temp.(C)	Channel	VIH_MIN	VIL_MAX	VIH_MIN	VIL_MAX
5.5	22	Q0	2.73	2.78	2.73	2.78
5.5	22	Q1	2.73	2.77	2.73	2.77
5.5	22	Q2	2.74	2.77	2.73	2.77
5.5	22	Q3	2.73	2.78	2.73	2.77
5.5	22	Q4	2.73	2.78	2.73	2.78
5.5	22	Q5	2.73	2.78	2.73	2.78
5.5	22	Q6	2.73	2.79	2.74	2.78
5.5	22	Q7	2.68	2.80	2.68	2.80
5.0	22	Q0	2.52	2.54	2.52	2.55
5.0	22	Q1	2.52	2.54	2.52	2.54
5.0	22	Q2	2.52	2.54	2.52	2.54
5.0	22	Q3	2.52	2.54	2.52	2.54
5.0	22	Q4	2.52	2.54	2.52	2.54
5.0	22	Q5	2.52	2.55	2.52	2.54
5.0	22	Q6	2.52	2.54	2.52	2.54
5.0	22	Q7	2.48	2.58	2.48	2.57
4.5	22	Q0	2.31	2.31	2.31	2.31
4.5	22	Q1	2.31	2.31	2.31	2.31
4.5	22	Q2	2.30	2.31	2.31	2.31
4.5	22	Q3	2.30	2.31	2.31	2.31
4.5	22	Q4	2.31	2.31	2.31	2.31
4.5	22	Q5	2.31	2.31	2.31	2.31
4.5	22	Q6	2.31	2.31	2.31	2.31
4.5	22	Q7	2.30	2.37	2.30	2.35

VI. Conclusions.

The 54AC273 exhibits shifts of no more than 30 mV in the clock threshold voltages following a total ionizing dose of 10 krad(Si).