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RADIATION HARDENED ELECTRONIC COMPONENT DEVELOPMENT AT GSFC

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ABSTRACT

Our experience at Goddard Space Flight Center (GSFC) is that a combination of Commercial-Off-The-Shelf (COTS) and radiation hardened technologies often provide the most cost effective solution for spaceflight applications. Limited availability of COTS components that satisfy certain spacecraft functions has led GSFC and others to develop radiation hardened versions for spaceflight use. This paper provides an introduction to some of these devices, including a high performance processor, mid and high rate on-board communication interfaces and an embedded processor/interface controller. A high density memory module is included because of the importance of bulk data storage to many spacecraft. Although the parts in it are not radiation hard, the module may be used in spaceflight due to a combination of testing and a system level error mitigation approach.

INTRODUCTION

Commercially available electronic components have often been used on Goddard Space Flight Center (GSFC) missions when they can be certified acceptable for flight. This usually involves upscreening the parts to spaceflight specifications to guarantee their acceptable operation in the launch and spaceflight environments. Some of the recent programs that have done this are the Solar Anomalous Magnetospheric Particle Explorer (SAMPEX) launched in 1991, the X-Ray Timing Explorer (XTE) launched in 1996, the Tropical Rainfall Measuring Mission (TRMM) due to launch this year (1997) and various other missions currently under development at GSFC. Spaceflight data on system performance has been presented previously[1].

The use of commercial technologies requires a system level approach to design[2]. Since commercial devices usually are adversely effected by radiation, consideration of this has to be taken into account to protect the spacecraft. Watchdog timers, error detection and correction circuitry and redundancy are some of the methods that can be used to minimize or eliminate these effects. Taking the system level approach to design has allowed GSFC to use commercial technologies to lower the cost of spacecraft.

The use of commercially available technology is not limited, however, to the use of commercial off-the-shelf (COTS) components from commercial vendors. Another important method is to incorporate commercial standards in the design of radiation hardened components. This allows the use of COTS equipment in the design and development of spaceflight electronic systems. Often COTS parts are able to serve as breadboard and Engineering Test Unit (ETU) versions of the flight article without modification or with minor modifications. COTS software and development tools can be used as well. The overall

advantage of this approach is to reduce the lower the cost, and still get the radiation hardness that's required.
The key to making this effort cost effective is to properly choose the pieces of the system that should undergo this radiation hardening. These pieces should be maximally integrated. That is, the highest level. of functionality as possible should be incorporated in them. The devices should be in areas of the system that may be maximally reused. Since there is a development effort required, we want to be able to utilize these components on as many spacecraft and in as many subsystems as possible to amortize the development cost. This also reduces the recurring cost for these devices after the initial development.

Among the functions that GSFC has indentified that meet these goals are high performance processors, mid and high rate on-board communication interfaces, embedded processing and high density memory. The rad hard solutions developed for these functions are the 32 bit Mongoose processor, the 20 Mbps Dual-Rate 1773 fiber optic data bus, the 1 Gbps Spaceborne Fiber Optic Data Bus (FODB) and the Essential Services Node (ESN). The radiation hardness of these components comes from a combination of radiation hard electronics fabrication processes with design principles minimizing the likelihood or effect of radiation. Well choosen trade offs between these options keep the cost of the development as low as possible while resulting in rad hard devices suitable for spaceflight. Due to the high cost and low densities of radiation hardened memories, the high density memory solution uses radiation tolerant memory chips in Irvine Sensors High Density Stacked DRAM modules. Radiation effects are removed at the system level.

GENERAL CONSIDERATIONS

Radiation hardness was not the only consideration in the choice and design of these pieces. Standards based on open architectures were used to maximize the interoperability of these devices. This also has the major benefit of allowing the use of COTS development tools for design, fabrication and test of the hardware and software systems. As was mentioned above, key pieces of spaceflight electronic systems were choosen to maximize the reuse of the devices after they were developed. A high level of integration ensured that the maximal benefit arose from the development effort. After all, if you're going through the trouble and expense of developing standard radiation hardened components for use on many spacecraft, it is advantageous to include as much of the common functionality as possible in the smallest package possible. This also promotes use across subsystems and spacecraft. The size, weight and power required by these functions is reduced. Schedules for spacecraft development are also reduced since some of the major components are available off the shelf. All these considerations have the effect of ultimately reducing the cost of spaceflight systems.

RADIATION EFFECTS

One of the most important differences between spaceflight electronics and terrestial electronics is the requirement to survive the radiation environment of space. There are non-spaceflight applications where radiation is also an important consideration, examples include nuclear power plants or weapons, but they are a relatively small part of the demand for electronic components and systems on the ground. In space, the requirement for radiation survivability is always a primary consideration.

Radiation effects are broadly separated into two categories, total ionizing dose and Single Event Effects (SEE's). TID effects are due to the cumulative effect of radiation impinging on the electronics. The result is a gradual degradation of the component over the lifetime of the mission. To some extent, all microelectronic components experience this effect. By balancing the radiation environment expected with the total dose radiation capability of a part, systems are built which tolerate almost any environment with an acceptable level of degradation through the mission lifetime. The tradeoff is usually that total dose

radiation hard components are more expensive, several generations behind their commercial counterparts and, often, slower and more power hungry.

SEE's are the result of a single particle upsetting a localized portion of a microelectronic circuit. Even though the initial effect is local, their ultimate effect can be spacecraft wide and catastrophic. SEE's occur in almost any part of any electronic component with differing degrees of probability, which will be discussed later, but it is instructive to use Random Access Memory (RAM) as an initial example of the wide range of possible effects. SEE's cause bit flips in RAM chips (for the moment assume there is no Error Detection and Correction - EDAC - in the RAM). If that RAM is just a minor data point, it will be a minor error and may not even be noticed. If the bit is important instrument scientific data, then the result could be a wasted data set. If the bit is in the program space or command storage space of the main spacecraft processor, a catastrophic spacecraft function could occur, or be prevented from occurring, which would result in the loss of the mission.

These are all examples of SEU's that cause "soft" errors. The error is a bit flip that may be reset if it is discovered. But there are "hard" errors that cannot be reset so simply. These type of errors cause the device to go into a state which requires power cycling to correct or the damage the device. One example is latchup, which may be destructive or non-destructive depending on the device. Other hard errors include burnout, gate rupture and dielectric rupture. The threshold at which an event occurs is the Linear Energy Transfer Threshold (LET). The higher the threshold, the more radiation hard the device.

MONGOOSE PROCESSOR

A commercial 80386 processor from Intel was used on the SAMPEX, XTE and TRMM spacecraft mentioned above. The 386 is a well known de-facto commercial standard. Software development tools are readily available from many vendors. Hardware development platforms consisted of 80386 based personal computers. The ability to use this off-the-shelf equipment reduced development costs signficantly. Through extensive ground testing and the addition of system radiation effect mitigation shemes[3], this processor was able to handle the radiation requirements of those missions. The 80386 design, however, has been eclipsed in the commercial sector by more advanced processors. Its level of integration is behind the currently available processors. The implementation of functions like the Dynamic Random Access Memory (DRAM) controller or the Floating Point Unit (FPU), for example, require peripheral chips. A more advanced spaceflight processor is needed for future spacecraft.

The solution developed at GSFC is the Mongoose V processor[4]. The Mongoose V is a commercially available, single chip, radiation hardened equivalent of the commercial R3000/FPU core developed by MIPS/LSI Logic. It's fabricated as a Honeywell Silicon On Insulator (SOI) HX2400 Gate Array. This gives it a Total Ionizing Dose (TID) hardness of at least 300Krad. It is latchup immune and has SEE LET_{TH} of 120 MeVcm^2/mg, which means it is effectively impervious to upset. It's "bulletproof".

The chip contains the MIPS/LSI processor core with FPU, instruction cache of 4K bytes, data cache of 2K bytes, Error Correction And Detection (EDAC) on the external bus, a Dynamic Random Access Memory (DRAM) controller and Dual Universal Asynchronous Remote Terminal (DUART). The cache speeds up the chips operation by keeping often used instructions and data in memory that can be accessed faster than the external memory. The EDAC, a Hamming code scheme, on the external bus allows the use of low cost, non radiation hardened memories instead of very expensive rad hard memories. The DRAM controller is critical for high speed data transfer. The Intel 8251 DUART allows for easy updating of software and monitoring of system performance during integration and test.

Early on in the design, the FPU was recognized as a critical requirement for Attitude Control Systems (ACS). The FPU was included in the Mongoose V to satisfy that need.

The Mongoose V processor is a good example of an easily identified key component of many spacecraft systems. Building this highly capable radiation hardened processor fulfills an obvious need within the spaceflight community. Since the processor is often the heart of the electronics system, it makes sense to make it as rad hard as possible. This avoids considerable complexity in the design and test of circuits to recover from radiation induced upsets. Guidance and control systems may safely rely on the processor to perform its mission critical tasks without concern for radiation induced upsets.

ESSENTIAL SERVICES NODE

The cost of developing a spacecraft is signficantly driven by the cost of the Integration and Test (I&T) phase. During this period, a large number of personnel test all the subsystem interfaces and functions to ensure that they can be safely and reliably connected together. Using standard interfaces to interconnect the subsystems can reduce the time required for this stage substantially. Simulation of the spacecraft interfaces for a subsystem can be done before arrival at the spacecraft using off-the-shelf simulators. These simulators can be used in I&T to verify correct subsystem operation before connection to the rest of the subsystems. The connection itself is easier since all subsystem interfaces are the same.

Additional savings are realized if the standard interface includes enough processing power to be an interface controller or embedded processor, as the situation warrents. This allows the device to be used in a great variety of designs. The functions that it performs can be determined by the software, so the part doesn't have to be redesigned for every mission.

The ESN consists of a multichip module (MCM) developed by GSFC in collaboration with Honeywell[5]. The processor in the ESN module is the UT69R000, 16 bit, 6 Mips, RISC processor. The primary interface is provided by a MIL-STD-1553/1773 protocol engine built into the module. This allows all the subsystems to connect together over a MIL-STD-1553/1773 data bus. Dual UARTs and 82C55 interfaces are also provided for point to point connections as well as software loading. Other features include a counter/timer, watchdog timer and serial and parallel inputs and outputs. A current source, 12 bit A/D and multiplexer circuitry is provided to sample analog voltages or thermistor telemetry points. The module is about 2.5" by 2.5" by 0.2". During normal operation it consumes about 1 W; in standby about 200 mW.

This part, like the Mongoose V, is highly radiation hardened. It will withstand at least 100Krad total dose. It will not latchup and has an LET_{TH} of greater than 30 $MeVcm^2/mg$.

AS1773 FIBER OPTIC BUS

Two types of data communications generally occur on spacecraft. There is the relatively low rate (< 20 Mbps) stream of commands to and responses from subsystems. There is also the high rate (>100 Mbps) data from some instruments. The first of these is dealt with using the AS1773 interface[6]. The AS1773 is a standard fiber optic bus that uses the same protocol as the MIL-STD-1773, but with the capability of running at 1 or 20 Mbps. A complete interface, called a terminal, consists of a protocol chip and two fiber optic transceivers. The protocol device is the ASCENT from United Technology Microelectronic Center (UTMC). The fiber optic transceivers are being developed by SCI and Boeing Defense and Space Group.

The protocol chip is fabricated on a process that ensures latchup immunity and an LET of 25 $MeVcm^2/mg$. The transceivers in both the Boeing and SCI components use rad hard chips for the signal processing circuitry inside the part. The choice of 1300 nm light for the fiber optic transmitters and receivers increases the radiation hardness of the devices significantly over the 850 nm used in the MIL-

STD-1773 that flew on SAMPEX and XTE[7]. In addition the data received is oversampled and a voting scheme used to mask out proton induced bit errors in the receiver.

The AS1773 transceivers, from SCI and Boeing, are part of the Microelectronics and Photonics Test Bed (MPTB)[8]. As part of this experiment, the AS1773 will be radiation tested in flight as well as on the ground. Portions of the ground testing of the Boeing transceiver have been completed[9]. A Bit Error Rate (BER) of less than 1E-10 is expected in spaceflight.

SPACEBORNE FIBER OPTIC DATA BUS(FODB)

Some communication links on spacecraft require rates in excess of the 20 Mbps that the AS1773 provides. Notable amoung these are instrument data collection rates for high rate instruments and memory transfers for large RAM memories. These applications require large amounts of data to be transferred quickly. Typically, rates of over 100 Mbps are required. This is clearly the realm of fiber optic systems. Reasons such as immunity to electromagnetic radiation, lower power and lower weight as compared to electrical systems have made fiber optics the choice for high rate commercial applications. This same reasoning applies to spacecraft systems.

The SFODB is a radiation hardened, fiber optic ring bus capable of transmission rates up to 1 Gbps. The Naval Research Laboratory (NRL), TRW, Motorola, Honeywell, DoD, and GSFC have been involved in its development[10]. The ring is redundant and cross-strapped. 1300 nm multimode fiber is used to provide the interconnections between the transceiver modules. These modules contain all the circuitry required for the SFODB interface. They are 2.2" x 2.7" x 0.3" multichip modules.

HIGH DENSITY MEMORIES

Radiation hardened memory chips are currently available from commercial vendors. These chips are especially well suited for uses such as processor instruction memories where a designer wants to be absolutely sure of the integrity of his data. However, the chips are expensive and, therefore, not so well suited to high density applications such as on board data storage. The number of chips in bulk data storage can be in the thousands, making the radiation hardened chips prohibitively expensive. In addition, the most dense chips available today are non-rad hard DRAMs. To get the most dense memory requires using these devices.

GSFC is currently using high density memory stacks of DRAMs built by Irvine Sensors. These stacks contain 160 Mb or 320 Mb, with more dense packages in the works. They've been used in SSTI/Lewis and the Hubble Space Telescope (HST) Solid State Memory (SSM). The chips used in them have undergone radiation testing, but are not radiation hardened[11]. They will have bit upsets in orbit. As a result, an EDAC code is used in conjunction with periodic scrubbing of the memory to detect and correct errors. It is at the system level that the radiation softness of these parts is overcome. As a result, much less expensive chips can be used and higher densities achieved.

CONCLUSION

The purpose of this paper has been to introduce some of the radiation hardened components that have been developed at GSFC for use in spaceflight. These devices perform general purpose functions required in most spaceflight subsystems. They have been specifically designed to encompass the needs of many spacecraft electronics boxes. The intention is to provide a high level overview to enable the reader to determine if these devices have applicability to their current and projected projects.

The devices described in this paper provide good examples of the various techniques available to radiation harden systems. The Mongoose V and ESN are examples of truly radiation hardened parts. The processes used to produce these devices are what make them rad hard. The AS1773 and FODB are a combination. These contain both rad hard and rad tolerant components, but intelligent component design has made them much harder than the parts that go into them. The high density memory uses radiation tolerant parts, but uses system level design to correct for the errors introduced. This continuum of solutions, using the radiation hardening techiques appropriate to each, is the best way to get the hardness required for spaceflight at a reasonable cost.

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