SEE and TID Characterization of an Advanced Commercial 2Gbit NAND Flash Nonvolatile Memory

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***Abstract*—An advanced commercial 2Gbit NAND flash memory (90 nm technology, one bit/cell) has been characterized for TID and heavy ion SEE. Results are qualitatively similar to previous flash results in most respects, but we also detected a new dynamic failure mode.**

***Index Terms*—CMOS, electronics, nonvolatile memory, radiation effects, single event effects, total ionizing dose.**

I. Introduction

We have tested commercially available Micron Semiconductor 90-nm 2-Gb NAND flash nonvolatile memory, both for total ionizing dose (TID) radiation damage, and for single event effects (SEE) from heavy ion exposure. These parts were obtained for $20 each. Commercially, nonvolatile flash memory sales now far exceed those of dynamic and static RAM (random access memory). Flash is very attractive for mobile, hand-held systems, such as iPods, digital cameras, and cell phones, because it can store large quantities of information, even with the power turned off. The features that make flash attractive in mobile systems also make it attractive for NASA systems. We have found a number of radiation issues, which would require significant effort to mitigate in a NASA system, but the results generally compare favorably with published results on older flash technologies, as might be expected with continued scaling. That is, total dose response would normally improve in more advanced parts, if oxides are thinner. And single event cross sections would be expected to shrink, with shrinking feature sizes. With these qualifications, results are generally what might be expected in an extension of previous studies, but we also detected a new dynamic failure mode, that has not previously been reported, to our knowledge.

II. Description of Devices

The test samples in this study were Micron Semiconductor 2Gbit nonvolatile flash memory, with 90 nm technology, and one bit/cell. The chips employ a NAND, or serial, architecture. In a NAND architecture, a large number of cells (typically 16 or 32) are connected in series, with a common drain connection to the bit line, and also a common source connection. In the alternative NOR architecture, there are many more source and drain connections, which allows faster access to individual cells. But the extra connections add an area penalty, and, for this reason, the cost per bit is higher for NOR chips. Typically, NOR flash is used to store operating code, and NAND flash is used for mass data storage. For additional discussion of flash architectures in general, see [1]–[4]. The external power supply is 3.3 V, where the higher voltage for programming and erase operations is achieved by means of an internal charge pump circuit. The chips come in a 48-pin TSOP (thin, small outline package), where the total package thickness was 1.5 mm. The plastic overlayer on top of the chip was determined to be 0.4 mm, by removing the plastic from one sample destroyed in testing. The chips have 2048 blocks of 1 Mbit each, of which the manufacturer guarantees that 2000 will be good, and the "bad" blocks are identified by the manufacturer. Each block has 64 pages, which are 2 K $\times$ 8. In our pre-radiation testing, the bad blocks usually performed flawlessly, but the manufacturer's in-house testing apparently revealed weak bits, that can give intermittent errors.

III. Test Procedures

These parts have been tested for TID (total ionizing dose), using the Co^{60} gamma source at Goddard Space Flight Center (GSFC), and SEE (single event effects), at the Michigan State University NSCL (National Superconducting Cyclotron Laboratory), and at the Texas A&M Cyclotron, and with protons at IUCF (Indiana University Cyclotron Facility).

A. Total Dose Testing

The Co^{60} source at GSFC is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.6. Time intervals for testing between exposures are also within the limits stated in 1019.6. Parts were under DC bias during exposures, but not actively exercised, because this corresponds to the actual operating condition during most of an extended space mission. These parts, and flash memory in general, are limited to 10^5 write/erase cycles, which typically take from a few seconds to a minute each. Therefore, the total time spent writing or erasing is a very small fraction of a multi-year mission. They can be read

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more often, but the system will not usually do multiple reads unless the stored information has changed.

For the first set of TID exposures (four parts), commands were given manually, but the second set of exposures (two parts) included an additional dynamic test mode. In the first set of four samples, two were programmed in a checkerboard initially, and tested in read-only mode. Between exposures, they were read, and errors (if any) counted, but they were not exercised in any other way. The other two parts were exercised in four patterns—all ones, all zeroes, checkerboard, and checkerboard complement—after each exposure. It was necessary to erase and verify that each device was erased between the programming of each pattern. The entire test sequence included multiple reads, multiple erases, and multiple programming steps. In these operations, the commands were given manually, meaning that (for example) "erase" was typed in on the computer, and the operator hit "Enter". Then the entire chip was erased at once. For this first set of exposures, operating frequency was 10 MHz (100 ns cycle time). After the first set of exposures, the parts were allowed to anneal at room temperature for about 90 hours, and then retested. In manual tests, they appeared to be fully functional, again. However, the parts were also subjected to an additional test mode, which we refer to as the dynamic test mode. In the dynamic test mode, each block was Read/Erased/Written, then the next block, and so on, with the commands generated by the test equipment. (We call this a dynamic test mode, because it was developed for dynamic SEE testing, meaning that we exercise the Read/Erase/Write functions with the beam on. When we do the same test between exposures in a TID experiment, we refer to it as dynamic, for convenience, but it is not truly dynamic, because it is not done in the Co-60 cell. In general, static tests will be those where the part is not exercised during the exposure, dynamic tests will be those where the part is exercised during exposure.) In this mode, errors were observed, which were not observed in unirradiated control samples. The second set of exposures (two parts) was conducted to investigate this effect, further. In addition to the dynamic mode, these parts were also exercised manually, as in the first exposures. In this second test, the operating frequency was 33.3 MHz (30 ns cycle time), which is the maximum specified by the manufacturer.

B. Single Event Testing

SEE testing was performed at the Michigan State NSCL, Texas A&M Cyclotron, and with 100 Mev and 200 MeV protons at IUCF. The heavy ion tests are summarized in Table I. Exposures were typically to 10^6 to 10^7 ions/cm^2, or 10^{10} or 10^{11} protons/cm^2. In all cases, total dose to the samples was monitored. Five test modes were used: (1) static—unbiased, where a pattern was written before exposure, and errors were counted after exposure, where no bias was applied during the exposure; (2) static, but with bias during exposure; (3) dynamic read, where the pattern was read continuously with the beam on, and errors counted; (4) dynamic read/write, where the initial pattern was continuously read and rewritten with the beam on, and errors counted; and (5) dynamic read/erase/write, where the initial pattern was continuously read, erased and rewritten with the beam on, and errors counted. The purpose of all the dynamic tests was to look for transient errors in the peripheral control circuits, especially during the high voltage erase and program steps. Power supply current was also monitored to detect latchup, but all exposures were at room temperature.

TABLE I
IONS USED IN TESTING

TAMU Ions	Energy/AMU	Energy (MeV)	Approx. LET on die (MeV•cm^2/mg)	Angle	Effective LET (MeV•cm^2/mg)
Ne	15	300	2.9	0	2.9
Ne	15	300	2.9	45	4.1
Ar	15	600	8.6	0	8.6
Ar	15	600	8.6	45	12.2
Kr	15	1260	28.8	0	28.8
Kr	15	1260	28.8	45	40.7
Xe	15	1935	55.6	0	55.6
Xe	15	1935	55.6	45	78.6
MSU Ions					
Xe^{136}	105	14280	25	0	25
Xe^{136}	70	9520	28.5	45	40

IV. RESULTS

A. Total Dose Results

A total of six parts were TID tested, and no failures were detected at 30 krad (SiO_2) or below, except that there were a few isolated single bit errors detected at some dose in an initial static read, that did not recur at higher doses. These errors were ones read incorrectly as zeroes, which is the opposite of what would normally be expected from radiation damage. We believe these errors are not due to radiation. The bits also functioned properly after being reset. At the 50 krad (SiO_2) level, five of the six parts had no errors, but the sixth part (which was exercised dynamically) had 2.9 million errors in the initial static read. These errors were reproducible, and did not change with clock cycle, until the bits were reset. After reset the bits all functioned properly, except that there was one intermittent bad bit—a one sometimes read as a zero. Neither this bit, nor any of the other intermittent bad bits, was in blocks flagged as bad by the manufacturer. At the 75- krad (SiO_2) level, four of the six parts (both read-only parts, one exercised manually, only, and one exercised both manually and dynamically) experienced total functional failure, because the erase function failed. That is, the parts worked at 50 krad (SiO_2), but not at 75 krad (SiO_2). After irradiation, these parts were read without error, and ones could be written to zeroes, but zeroes could not be erased to ones. The two remaining parts experienced the same failure mode, after the next dose increment, which was to 100 krad (SiO_2).

The first four parts were allowed to anneal at room temperature for about 90 hours, and retested. In static tests, the parts appeared to be fully functional again, even the erase function. However, when they were exercised dynamically, with the read/erase/write commands given under computer control, there were large numbers of errors. The second set of exposures was done to investigate this result further. When the second set of samples was annealed for a few days after irradiation, the same result was obtained, except that one bit on one sample did not fully recover. It could be written as a zero, or erased to a one, but in a checkerboard pattern, it ended up as a zero instead of a one.

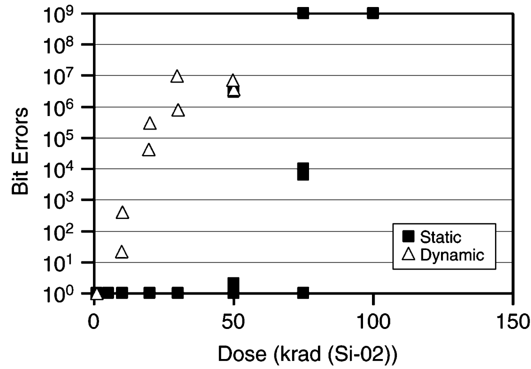

Fig. 1. Dynamic and static error rates compared, with dynamic errors starting at much lower doses.

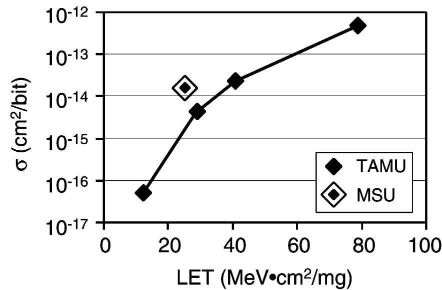

Fig. 2. Static SEU cross-section.

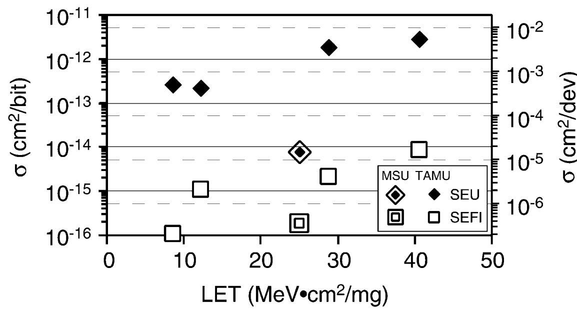

Fig. 3. Dynamic read error cross section. SEU cross sections are on the left axis, SEFI cross sections on the right.

The results of the dynamic testing were that there were no errors in either part before irradiation. Results after irradiation are shown in Fig. 1. There were a few errors, even at the first exposure level, but the number of dynamic errors increases rapidly with dose, to several million before failure. These numbers were stable through multiple cycles, and also with slower clock speeds. At every level, however, the bits could be read correctly if the commands were given manually, as we have already explained. We will discuss the reasons for this result later.

B. Single Event Results

In the heavy ion SEU testing, errors were seen for all LETs and all bias/operating conditions. Results are shown in Figs. 2–5. In all cases, the All-0's was found to be the worst-case pattern, so after the first few runs, all subsequent runs were carried out with this pattern.

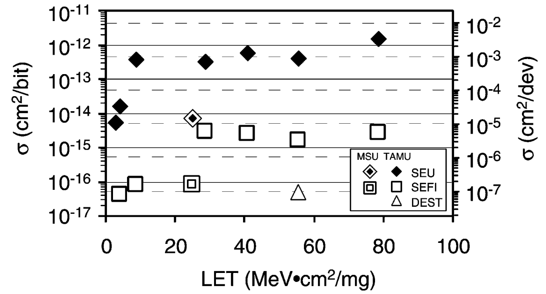

Fig. 4. Dynamic Read/Write error cross-section, for single bit errors, SEFI, and destructive effects (SEU on the left axis, other effects on the right).

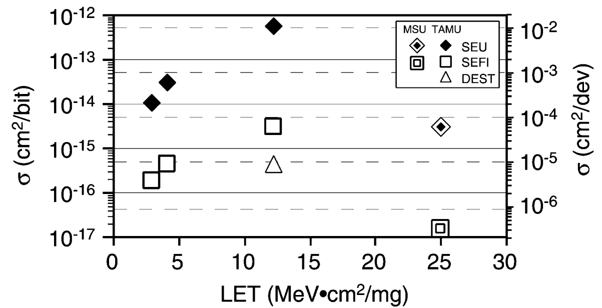

Fig. 5. Dynamic Read/Write/Erase error cross section, for single bit errors, SEFI, and destructive effects (SEU on the left axis, other effects on the right).

Even for the unbiased and static cases, in Fig. 2, bit errors and Page/Block errors were evident in the patterns of upsets observed. By page and block errors, we mean that all or most of the bits in either a page or a block were detected as errors. It is likely that the Page/Block errors arise due to upsets in configuration registers in the memory array, rather than upsets of the individual bits. For this reason, the page and block errors have been removed from the bit error cross-section in Fig. 2. In these tests, the sample was read only before and after the exposure, but not during the exposure. For this reason, it could not be determined exactly when the errors occurred. It is likely that a small fraction of the individual bit errors were obscured by page and block errors, so cross sections are approximate for unbiased and static error modes.

For the Dynamic Read condition, in Fig. 3, the parts exhibited other Single Event Functional Interrupts (SEFIs) in addition to the bit and Page/Block errors. (Page and block errors are counted as SEFIs in Fig. 3–5, but there were also other kinds of SEFIs. In general, SEFI is used to mean any non-destructive interrupt—something stopped working, but operation was eventually restored.) Here, and in the following discussion, SEU cross sections will be given in cm^2/bit, while SEFI and destructive event cross sections will be normalized on a per device basis. For Dynamic Read/Write, in Fig. 4, and Dynamic Read/Erase/Write, in Fig. 5, functional failures (destructive events) were observed that made it impossible to Erase or Write to the memory. Page/Block and SEFI errors were not identified in some cases, because of the functional failure of the device. Generally, SEFIs and functional failures occurred at roughly comparable rates. SEFIs that were detectable (because the chip survived) are plotted in Figs. 3–5. We were not able to do destructive physical analysis (DPA) to determine the

cause of these functional failures, but they are probably due to Single Event Gate Rupture (SEGR). SEGR was first identified by Blandford *et al.* [5], in nonvolatile memories during high-voltage write and erase operations.

In addition to the above errors, stuck bits were seen during testing. (Stuck bits were first identified by Koga *et al.* [6], as bits that could not be programmed into one state or the other, in SRAMs. It was argued by Dufour *et al.* [7] that this effect was due to interactions of single ions, based on experimental evidence. Further analysis, first by Oldham *et al.* [8] and later by Poivey *et al.* [9] has tended to confirm this conclusion. Basically, the idea was that an ion, passing through the gate of a transistor, deposits a high density of charge in a small region (micro-dose), which causes a threshold voltage shift, which leads to leakage current. Then there is a node in the cell that cannot be charged to high voltage, because charge leaks away as fast as it can be added. For a review, see also Oldham and McLean [10].) These apparently tended to anneal rapidly (a timescale of minutes), although a few bits seemed to be persistent. In a flash cell, micro-dose damage would be expected to anneal rapidly, because of the thin tunnel oxide, which is consistent with the observations. The relatively few persistent stuck bits are probably due to a leakage path from damage to the oxide, an idea which has been discussed by Paccagnella, and others [11]–[15]. The persistence of these stuck bits beyond the time of testing could not be investigated due to the functional failure of the die on which they were observed.

In the proton tests, no static single bit errors were observed. There was a low incidence of dynamic read errors, where transient current pulses in the read circuit caused a low current (zero) to be mistaken for a high current (one), but the contents of the bits were not altered. There was also one SEFI, where the chip would not respond to commands for a time. Other errors, involving large numbers of bits, happened only when the accumulated total dose was close to the failure level for the technology. These errors were probably due to TID, rather than SEE.

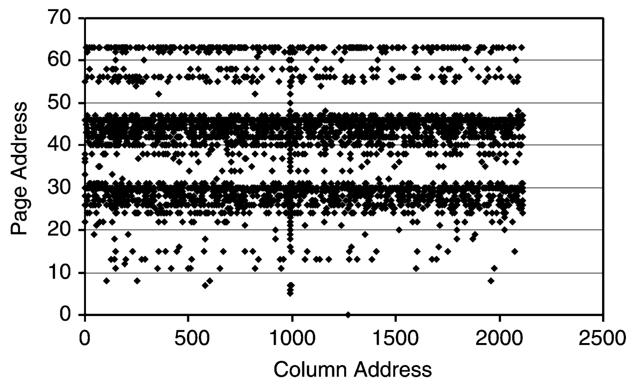

Fig. 6. Bit error map for initial static read, at 75 krad (SiO_2). Non-random distribution indicates problems in peripheral circuits, rather than individual bits. Page address is also the row number.

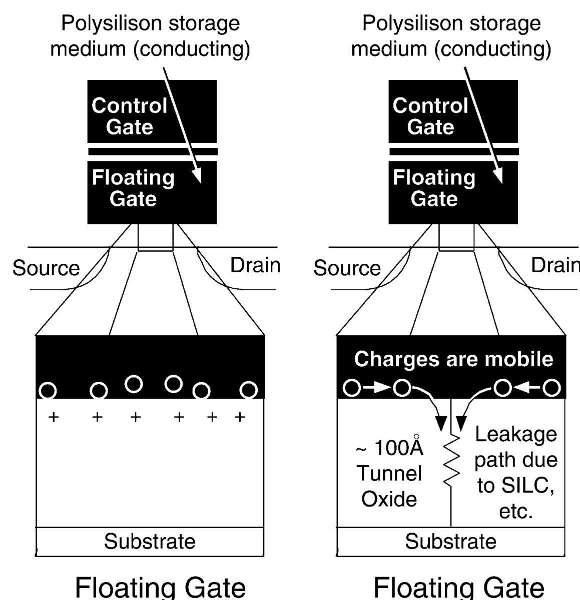

Fig. 7. Radiation damage mechanisms: (a) positive oxide charge; (b) oxide damage along an ion track, leading to a conducting path in the oxide.

V. Discussion

A. TID Discussion

Nonvolatile memory is a critical need for many NASA systems, and there are a number of previous reports on the radiation response of nonvolatile CMOS memory, from previous technology nodes [16]–[18]. To our knowledge, this is the first such report at the 90 nm technology node, however. We observe qualitative similarities with the earlier work on older technology nodes, in some respects, and differences in others. Total dose failures have been reported in other flash at 8–14 krad [17], [18], because of the failure of the high voltage charge pump circuit. Here the failure level is above 50 krad, even in a short, high dose rate exposure. Annealing could not be studied in detail, but it appeared to be relatively rapid, which suggests that in a low dose rate space environment, the failure level would be much higher. The radiation damage would anneal, almost as fast as it was created. It is well known, that oxide thickness is reduced with continued scaling, and that thinner oxides are more radiation-resistant, so a higher failure level would be expected for this technology. Although we do not have detailed process information for these chips, advanced flash memories [4], [19] typically have (only) a 7–10 nm tunnel oxide, which would explain rapid annealing, by the usual tunneling process [20]. Although the failure of the charge pump for the erase process is the limiting factor in the TID environment, it is not the only failure mechanism. In Fig. 2, two parts have about 10^4 bad bits in an initial static read at 75 krad. However, a bit error map for one of these is shown in Fig. 6, and the errors are concentrated in certain rows. The page address is also the row number, which is the same as the word-line number. This suggests that these errors are due to the peripheral circuits for these rows, and not due to the failure of individual bits.

In current flash technology, the cells are n-channel transistors, where the floating gate is filled with electrons in the zero state, and empty of electrons in the one state. Since the effect of radiation is to introduce positive charges into the oxide, radiation tends to turn zeroes into ones, but not the reverse [as illustrated in Fig. 7(a)]. In the heavy ion tests, all the single bit errors were zero-to-one errors. In the TID tests, bit errors were predominantly zero-to-one at high doses. At low doses, there were occasional errors of the wrong polarity, which were also

intermittent, meaning that they disappeared at the next higher dose. Our view is that these were probably not due to radiation, but it is possible to get errors of both polarities in the TID test. We note that these chips do not have built-in error correction, but the manufacturer recommends that error correction be used (off chip), because it is difficult to keep the error rate below one part per billion without it, even in the absence of radiation. Error correction would be expected to eliminate most of the single bit static errors, which is the main effect in Fig. 2.

The errors detected in the dynamic read/erase/write test mode, after TID exposure, appear to be new error mechanism—at least we are not aware of it having been reported before in radiation tests. Basically, the pattern is read, block by block, and compared to an "expected" pattern, which is the complement of the actual pattern. Every bit, then, is detected as an error, which is then corrected, in principle, by erasing and reprogramming. The results are that the read and erase steps are done correctly, but the reprogramming step is not completely successful, with the error count running to several million at higher doses, as shown in Fig. 1. These errors do not depend on the clock cycle time, because increasing the cycle time by $2\times, 4\times$, or $8\times$ had no effect on the number of errors. If the same commands are given manually, the entire memory is read, then erased, the reprogrammed, rather than going block-by-block, and no errors are observed. We returned two of these parts to Micron, and their product assurance group duplicated our results. They found that, in some cases, when one block is selected to be erased, the adjacent word line is also selected (incorrectly). The bit error map in Fig. 6 is consistent with this idea—errors are concentrated in certain rows, and are not randomly distributed. Then the block adjacent to the selected block is also erased, or partially erased, which causes the observed errors. This coupling between word lines was not observed in all blocks, and it was not observed at all before irradiation, but it could limit the use of the part in a space system. We note that we have done TID testing of one other 90 nm NAND flash memory, which will be reported in full later, but it did not have this same kind of dynamic error mode.

It should be mentioned that unintentional disturbances of adjacent cells are an important reliability concern for NAND flash, even in the absence of radiation. For example, if a cell is selected to be programmed (written), both its word-line and bit-line are selected (on). But because of the serial nature of the NAND architecture, many other cells are half-selected, meaning that either the bit-line or the word-line is on, but not both. Manufacturers normally invest significant design effort, during product development, in making sure these half-selected cells are stable against unintended disturbances (for reviews of this topic, see [4], [21]). But in our tests, the dynamic errors are not due to disturbances of half selected cells—both the bit-line and word-line are on, when the word-line is supposed to be off.

B. SEE Discussion

In the SEE results in Figs. 2–5, a number of error mechanisms are reported, with cross sections. These errors are qualitatively similar to previous reports. For example, the same mechanisms are reported in [16] for older technology, but the cross sections in Figs. 2–5 are generally two or more orders of magnitude lower than those in [16], 10^{-5} cm^2/device or less, compared to 10^{-3} cm^2/device or more. Although there may be significant issues in using these parts in a space system application, they are still attractive, because there may not be a better alternative. We note that we have fitted a Weibull curve to the upset data in Fig. 2 (threshold at $\text{LET} = 12$, width $\text{LET} = 68, \text{exponent} = 3$, and saturation at 5×10^{-13} cm^2/bit). For these parameters and the Adams Ten Percent Worst Case environment, CREME96 [22] calculated an error rate of 1.5×10^{-16} errors/bit-day. For a chip with two billion cells, this is equivalent to one chip error about every 9000 years—good enough for many space systems

The most common error in heavy ion testing is a single bit error, zero turned to one, when the ion passes through the floating gate. Positive oxide trapped charge, compensating the negative charge on the floating gate, is indicated schematically in Fig. 7(a), which is an attractive idea because of its simplicity. However, the actual physical charge loss mechanism, in a heavy ion strike, is more complicated, and it has been described in a number of previous reports [23]–[25]. Oxide damage from the ion strike, leading to a low resistance leakage path, as illustrated in Fig. 7(b), has been reported previously [24], [25], but it is not the focus of this work.

VI. Conclusion

We have tested an advanced commercial 2 Gb NAND flash memory from Micron Semiconductor, in both TID and heavy ion environments. Results compare favorably with earlier reported results on older flash technology, with higher total dose tolerance, and typical SEE cross section two or more orders of magnitude smaller than for older flash technology. However, there are a number of issues that would still have to be addressed before these parts can be used in space systems, including the dynamic error mode we have described.

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