Synopsis V7.0
Total Ionizing Dose Testing of the
Intel Pentium III (P3) and AMD K7 Microprocessors[†]

Jim Howard[1], Ken LaBel[2], Marty Carts[3], Ron Stattel[3],
Charlie Rogers[3], Tim Irwin[4] and Zoran Kahric[5]

1. Jackson and Tull Chartered Engineers, Washington DC 20018
2. NASA GSFC, Greenbelt, MD 20771
3. Raytheon ITSS, Greenbelt, MD 20771
4. QSS, Inc., Greenbelt, MD 20771
5. Orbital Sciences Corp., Dulles, VA 20166

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Introduction

As part of the Remote Exploration and Experimentation Project, work was funded for the "Radiation Evaluation of the INTEL Pentium III and Merced Processors and Their Associated Bridge Chips." As another step in the completion of this work, Intel Pentium III (P3) and AMD K7 processors were tested at the Indiana University Cyclotron Facility (IUCF) and the GSFC Radiation Effects Facility (REF) for total dose effects. The primary purpose of this testing was to evaluate the P3 and K7 Devices Under Test (DUT) for their susceptibility to ionizing radiation dose. A secondary objective was to determine if the DUTS would have accelerated degradation if exposed to a displacement damage producing radiation source, such as the proton beam at IUCF. The remainder of this report details the test process, methodology and results from this total dose testing.

Devices Tested

Pentium III devices with rated clock speeds ranging from 550 to 1 GHz were tested. Pentium III devices were manufactured by Intel and K7 devices were manufactured by Advanced Micro Devices. All devices were characterized prior to exposure. A listing of all devices used in this testing is given in Table I (Pentium III devices) and Table II (AMD K7 devices) below.

Test Facility

Facility: Indiana University Cyclotron Facility (IUCF)
Protons: 198 MeV **Flux:** 10^6 to 10^9 protons/cm^2/s.
Facility: GSFC Radiation Effects Facility (REF)
Gammas: Cobalt-60 **Dose Rates:** 3 to 10 krads(Si)/day.

Test Methods

Temperature:

The test was conducted at room temperature. Intel P3 junction temperature was monitored using an on-die diode (not available on the K7 die).

[†] This work was performed at NASA/GSFC for the Remote Exploration and Experimentation Project. This project is part of NASA's High Performance Computing and Communications Program, and is funded through the NASA Office of Space Sciences.

TABLE I
Pentium III DEVICE UNDER TEST (DUT) TABLE

Device	Vendor	Rated Speed	Test Condition	Package	Source	Package Markings
Pentium III	Intel	800 MHz	Biased	SC242	Co-60	800/256/100/1.65V S1 90240169-0091 MALAY imc '99 SL457
Pentium III	Intel	933 MHz	Biased	SC242	Co-60	933/256/133/1.7V S1 11040081-0488 Phillippines imc '00 SL4KK
Pentium III	Intel	550 MHz	Unbiased	SC242	Co-60	550/256/100/1.65V S1 90050493-0307 MALAY imc '99 SL3V5
Pentium III	Intel	650 MHz	Unbiased	SC242	Co-60	650/256/100/1.65V S1 10160248-0411 PHILIPPINES imc '99 SL452
Pentium III	Intel	650 MHz	Unbiased	SC242	Co-60	650/256/100/1.65V S1 10160260-0075 PHILIPPINES imc '99 SL452
Pentium III	Intel	700 MHz	Unbiased	SC242	Co-60	700/256/100/1.65V S1 90160187-0060 MALAY imc '99 SL454
Pentium III	Intel	850 MHz	Unbiased	SC242	Co-60	850/256/100/1.65V S1 10280400-0262 Philippines imc '99 SL47M
Pentium III	Intel	933 MHz	Unbiased	SC242	Co-60	933/256/133/1.7V S1 00280415-0068 COSTA RICA imc '99 SL47Q
Pentium III	Intel	650 MHz	Biased	SC242	Protons	650/256/100/1.65V S1 10100418-0161 PHILIPPINES imc '99 SL3KV
Pentium III	Intel	550 MHz	Biased	SC242	Protons	550/256/100/1.65V S1 90050493-0099 MALAY imc '99 SL3V5
Pentium III	Intel	650 MHz	Biased	SC242	Protons	650/256/100/1.65V S1 10100418-0293 PHILIPPINES imc '99 SL3KV
Pentium III	Intel	700 MHz	Biased	SC242	Protons	700/256/100/1.65V S1 90160187-0108 MALAY imc '99 SL454
Pentium III	Intel	700 MHz	Biased	SC242	Protons	700/256/100/1.65V S1 90160187-0055 MALAY mc '99 SL454
Pentium III	Intel	700 MHz	Biased	SC242	Protons	700/256/100/1.65V S1 90160187-0057 MALAY imc '99 SL454
Pentium III	Intel	750 MHz	Biased	SC242	Protons	750/256/100/1.65V S1 90260050-0092 MALAY imc '99 SL456
Pentium III	Intel	850 MHz	Biased	SC242	Protons	850/256/100/1.65V S1 10280400-0071 Philippines imc '99 SL47M
Pentium III	Intel	850 MHz	Biased	SC242	Protons	850/256/100/1.65V S1 10280400-0293 Philippines imc '99 SL47M
Pentium III	Intel	850 MHz	Biased	SC242	Protons	850/256/100/1.65V S1 10280400-0308 Philippines imc '99 SL47M
Pentium III	Intel	933 MHz	Biased	SC242	Protons	933/256/133/1.7V S1 00280415-0224 COSTA RICA imc '99 SL47Q
Pentium III	Intel	933 MHz	Biased	PGA370	Protons	933/256/133/1.7V L045A581-0194 SL4ME
Pentium III	Intel	933 MHz	Biased	SC242	Protons	933/256/133/1.7V S1 11040081-0098 Phillippines imc '00 SL4KK
Pentium III	Intel	1 GHz	Biased	PGA370	Protons	1000/256/133/1.7V Q112A279-0442 SL4MF
Pentium III	Intel	1 GHz	Biased	PGA370	Protons	1000/256/133/1.7V Q111A242-0067 SL4MF
Pentium III	Intel	650 MHz	Unbiased	SC242	Protons	650/256/100/1.65V S1 10100418-0176 PHILIPPINES imc '99 SL3KV

Test Hardware:

The system hardware consists of two subsystems, the PXI Test Controller and the DUT Computer subsystems. Any cabling not required for the operation of the DUT computer is considered part of the Test Controller subsystem. Figure 1 illustrates the overall test configuration for biased irradiations. This is not substantially different from the configuration used for Single Event Effects (SEE) testing.

For unbiased irradiations, the setup is similar but the DUT computer resides outside the irradiation area. Also available to both test setups is an FPGA-based timer card. This timer card is plugged into the DUT's motherboard ISA bus. When used with the biased

DUT, the Cobalt-60 shutter is down during the collection of the data, and is then removed afterwards to prevent damage due to irradiation.

The PXI Test Controller and the DUT Computer subsystems are described below. Following that is a description of the DUT processors.

TABLE II
AMD K7 DEVICE UNDER TEST (DUT) TABLE

Device	Vendor	Rated Speed	Test Condition	Package	Source	Package Markings
K7	AMD	600 MHz	Biased	SC242	Protons	AMD-K7600MTR51B C 219949147583
K7	AMD	650 MHz	Biased	SC242	Protons	AMD-K7650MTR51B A 210017540094
K7	AMD	700 MHz	Biased	SC242	Protons	AMD-K7700MTR51B A 210019614073
K7	AMD	900 MHz	Biased	SC242	Protons	AMD-K7900MNR53B A 210036542751
K7	AMD	1 GHz	Biased	SC242	Protons	AMD-K7100MNR53B A 710026014044
K7	AMD	1 GHz	Biased	SC242	Protons	AMD-K7100MNR53B A 710026147861
K7	AMD	650 MHz	Unbiased	SC242	Protons	AMD-K7650MTR51B A 230015009833

PXI Test Controller Subsystem

The PXI Controller, as shown in Figure 2, resides outside the irradiation chamber, removed from the DUT subsystem by about 45 feet of cabling. It consists of the PXI components and the PXI Controller to DUT Computer cabling.

The PXI components include the PXI chassis, which contains an embedded controller (running Win98 or WinNT (both were used at various times), Labview™ (LV) environment, and a custom LV application), a signal switch matrix, and two digital multimeters (DMMs) in the voltage measurement mode. The switch matrix provides two functions: The multiplexing of analog signals to one of the DMMs, and contact closures (pulling signal levels to ground). The other DMM is dedicated to monitoring one specific analog value and measuring that without regular periodically switching, so that it may measure more frequently with less delay. Figure 2 shows additional details of this switching and measurement functionality.

Other PXI Controller components include user interface (keyboard/monitor/mouse), network connectivity and AC power conditioning (which supports both the PXI Computer and the DUT Computer).

Most of the PXI Controller to DUT Computer cabling leaves the PXI subsystem from the switch matrix (described further below). Exceptions are the AC power cable to power the DUT computer, a serial (RS-232) cable for telemetry/command of the DUT Computer (telemetry originates within the DUT Computer, commands originate within the PXI Controller) and the DUT Computer's keyboard/monitor/mouse extensions.

The Goddard Space Flight Center's Cobalt-60 Radiation Effects Facility is an in-air exposure cell. Devices to be irradiated are set up in a room at the chosen distance from the Co-60 source. The room is secured, and a thick Lead (Pb) shutter is hydraulically raised to expose the devices to be tested. By means of a shielded window (for observation) and a thick concrete wall, the cell is separated from the user area. Sub-floor 4" curved pipes allow for cabling to penetrate into the irradiation cell. The PXI computer is located in the user area, close to these pipes.

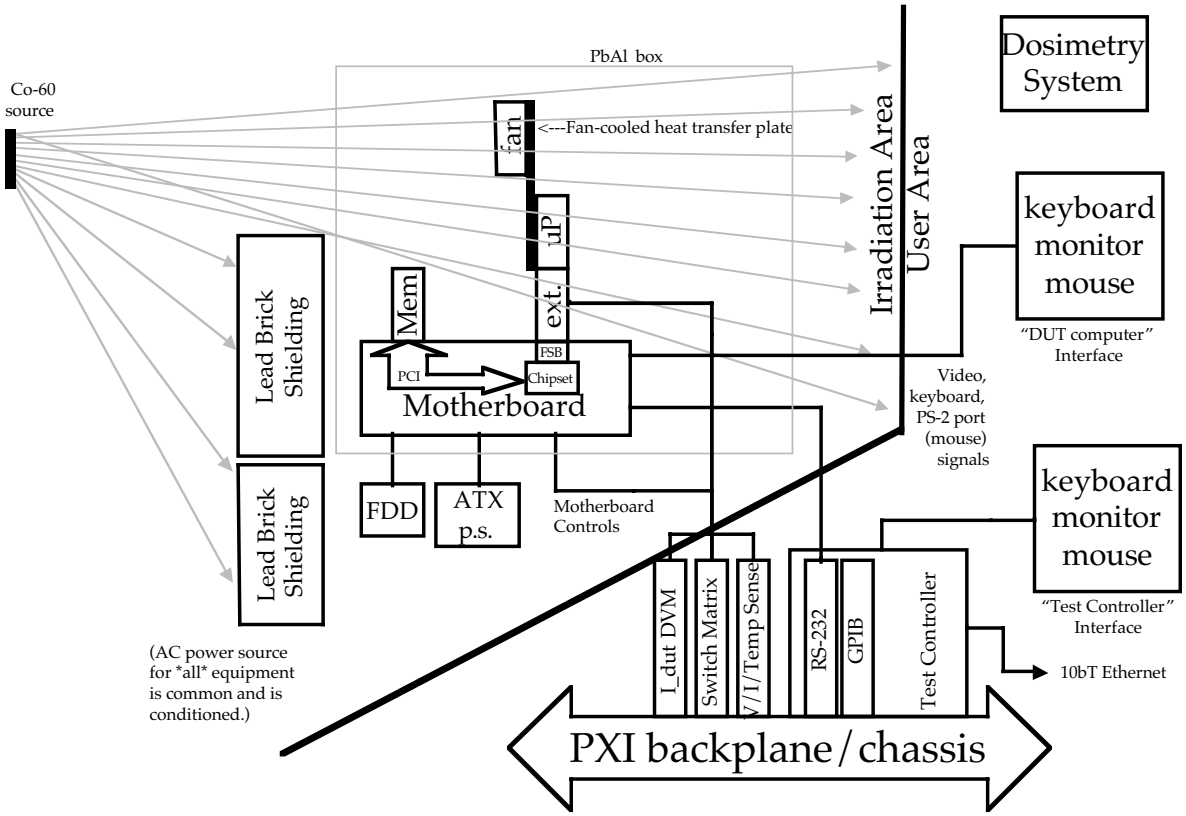

Figure 1. Overall block diagram of biased TID test, showing shading and shielding elements.

DUT Computer Subsystem

The DUT computer subsystem for biased irradiation (differences for the unbiased irradiations are described at the end of this section) resides within the irradiation cell, and inside a Lead-Aluminum (PbAl) box to moderate the spectrum of the gamma rays. A serpentine baffle allows for the entrance of cabling to the box. The motherboard stands vertically, planar with the center of the Co-60 source. The DUT, on an extender card, sticks out horizontally from the motherboard, with the die facing the source. Video card and memory modules also stick out from the motherboard, but lead bricks stacked immediately outside the PbAl box are employed to reduce the dose exposure of all components except the DUT. (Nonetheless, dosing is not eliminated and mortality of these components is a continuing issue in the testing. Multiple motherboards, memory modules and video cards have lost functionality in the pursuit of the total dose limit of the DUT processors.)

The DUT computer subsystem consists of the components immediately concerned with the operation of the DUT computer. These include components mounted directly to the motherboard and components located nearby (i.e. floppy disk drive, ATX power supply, and the computer side keyboard/monitor/mouse extension box). Note: ATX describes electrical and physical aspects of motherboard, power supply and other components of ATX form-factor computers, which includes most desktops in use

during this project. These components are connected with ~6′ extensions and are located and shielded for minimum dosing.

Directly attached to the commercial motherboard are the modified DUT processor (described later in the Pentium III section) on top of a DUT processor extender card, a RAM module (DIMM) and the video card.

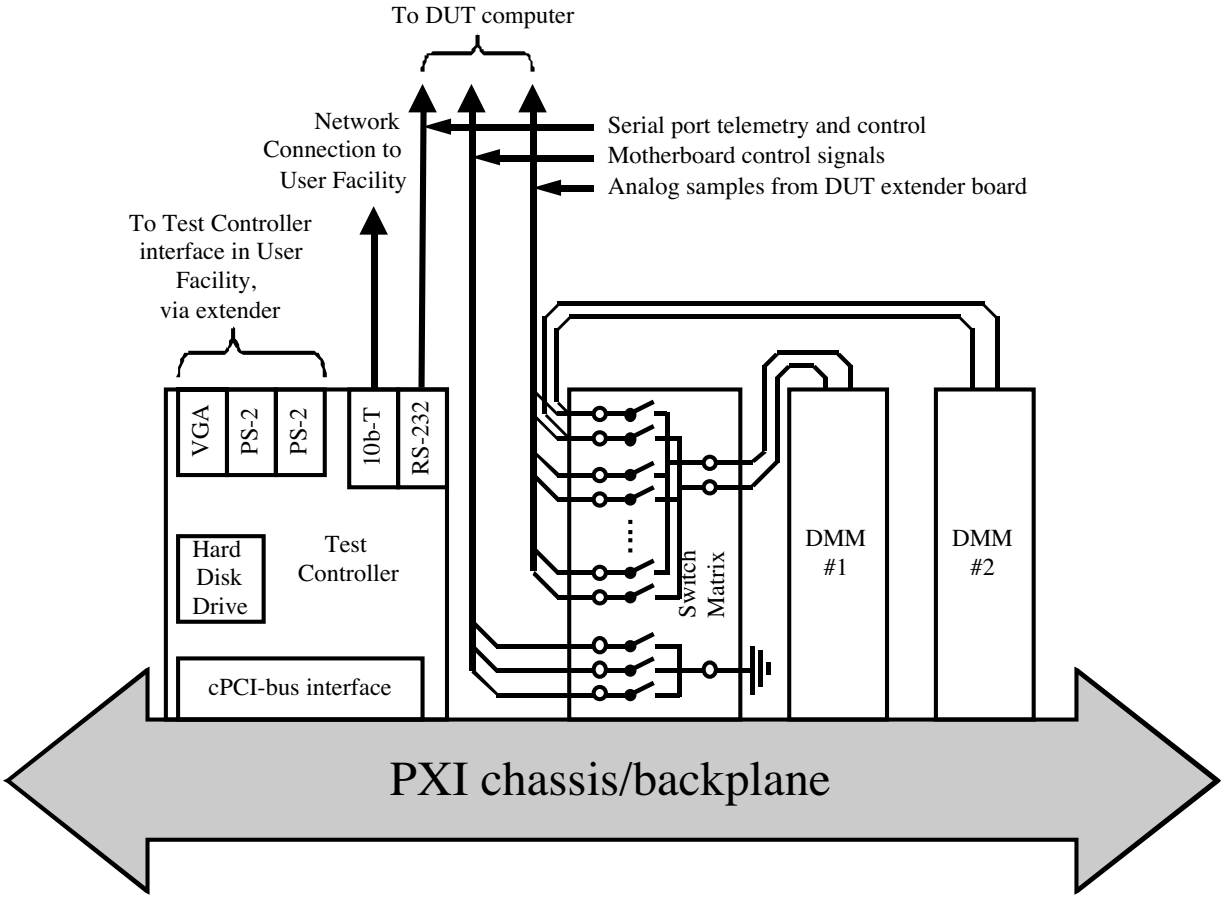

Figure 2. Block diagram of the PXI subsystem.

The DUT processor extender card is inserted between the DUT processor and the motherboard, extending the 242 DUT processor card edge contacts an additional 1.5″ above the motherboard. This is done for two reasons. First, it allows for greater shading of the motherboard and other components not intentionally being irradiated. Second, the extension provides the best opportunity for monitoring DUT currents and voltages.

A simple extender board was modified to insert a low resistance in series with the power traces. The schematic of the voltage and current sampling shown on the left of Figure 3 is duplicated three times on the extender card to monitor the three supplies applied to the processor card. Also shown, on the right of Figure 3, is the P3 temperature sensing diode, driver, and monitoring circuit schematic. Twisted shielded cabling is added to monitor these developed voltages. A photograph of the modified extender card can be seen in Figure 4.

Intra-DUT computer cabling includes the floppy disk drive cable and extension, an extension cable for the ATX and the keyboard/monitor/mouse extension (a CAT5 cable based extender from Cybex, Inc.).

The motherboard is modified to allow connection to two controlling digital signals, both of which are momentary contact closures. The motherboard front panel power on/off (MotherPonoff) input signal which is normally connected to a momentary pushbutton on the front panel of a desktop computer is controlled by the PXI switch matrix, as is the motherboard front panel soft reset (MotherSR) input signal.

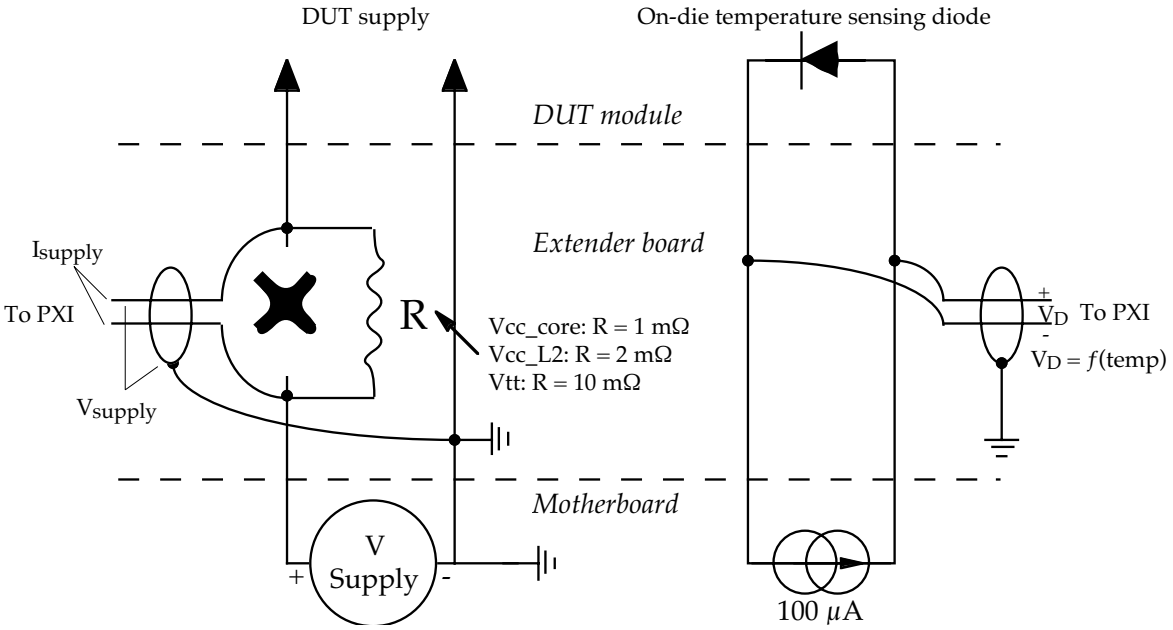

Figure 3. Schematic diagram for the DUT extender card.

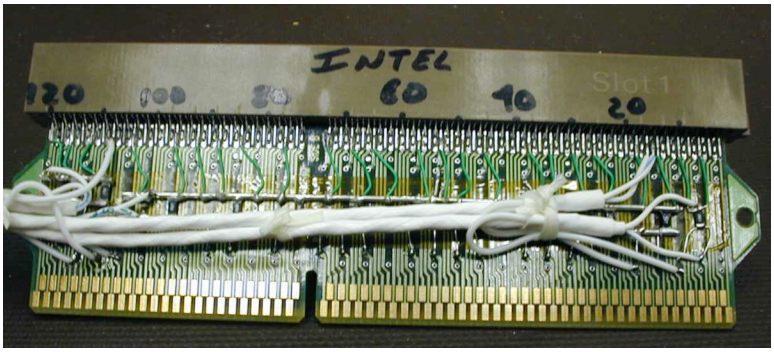

Figure 4. Photograph showing the processor extender card.

ATX PS on/off state is normally controlled by a constant signal from the motherboard (The ATX SP supplies a standby +5V to power this motherboard function). This signal (PS_ON#) is, approximately, a latched toggle of the front panel signal, MotherPonoff. This motherboard < -- > PS PS_ON# connection is modified—The line is cut so that the ATX power supply's PS_ON# input can be controlled directly from the PXI. This additional control is necessary because the computer can hang to the

extent of not responding to the normal on/off commands. The ATX PS AC power is extended back to the user facility.

The DUT Computer runs a real-time operating system and an autoboot software application residing on floppy disk, which periodically reports to the PXI through the motherboard's serial port via a null modem cable (see the section, Test Software, for details). Commands are also input from the PXI Computer over this cable.

Three previously described digital control signals, MotherPonOff, MotherSR and PS_ON#, leave the DUT Computer subsystems via shielded cable. Four twisted shielded pairs carry current/voltage samples from the DUT processor extender card to the PXI subsystem. The length of this cabling can be at least as long as 45' without compromise of signal quality.

An ISA timer/interrupt generator board was developed because of the need of having an external timing source. To save cost and schedule impacts, an ISA printed circuit board was acquired for another project and modified. What made the process relatively easy was that the board had a programmable Field Programmable Logic Array (FPGA) as the ISA interface. We developed a custom design for the FPGA (Actel 1020) and programmed the FPGA with our custom features. This gave the group a very cheap way of developing a simple external timer board.

The problem of the ISA board is the slow ISA clock gave marginal sample timing. ISA bus clock signal run at 8 MHz. This gave us sufficient timing source to accomplish our testing.

The basic features of the timer board were to either count up until read and reset or generate interrupt to the process at a known rate.

The ISA board that was developed for this project supported the following features

- A 16-bit counter that is clocked at the ISA clock rate (8Mhz).
- A 16-bit hold counter that can save the current count until read.
- Single command to lock the save the current count. This is used because it takes two cycles to read the count. To get better time precision we clock the current time into a buffer and then read the buffer.
- Two 8 bit registers can be read as a 8 bit read or a 16 bit read..
- Ability to clear the active count
- Ability to load the current count.
- Generate interrupts on reaching a terminal count
- Clear Interrupts

If a future board were developed it would be recommended to make it a PCI bus board. This would give much better timing. The PCI bus clock can be run up to 133Mhz.

This custom FPGA card block diagram is shown in Figure 5. The timer board was set up to provide an interrupt every 16383 cycles of the ISA bus clock. This information is used within test H (as described in the software section) to determine if any timing delays occur that would indicate a degradation of the processor due to dose.

Occasionally, the irradiation shutter was closed and the timer card inserted into an ISA slot on the biased motherboard to take this data for the biased tested parts as well. When not in use in the biased DUT test, the timer card resides in the unbiased test setup.

For unbiased irradiations, as many as four DUTs are inserted into an assembly with four all-pins-grounded sockets, and positioned within a PbAl box identical to that used for the biased irradiations. Periodic measurements involve removing the DUT grounding assembly from irradiation, inserting each DUT in turn into an identical DUT

computer as was previously described (except that it resides outside the irradiation area) and making functionality and timing measurements on them.

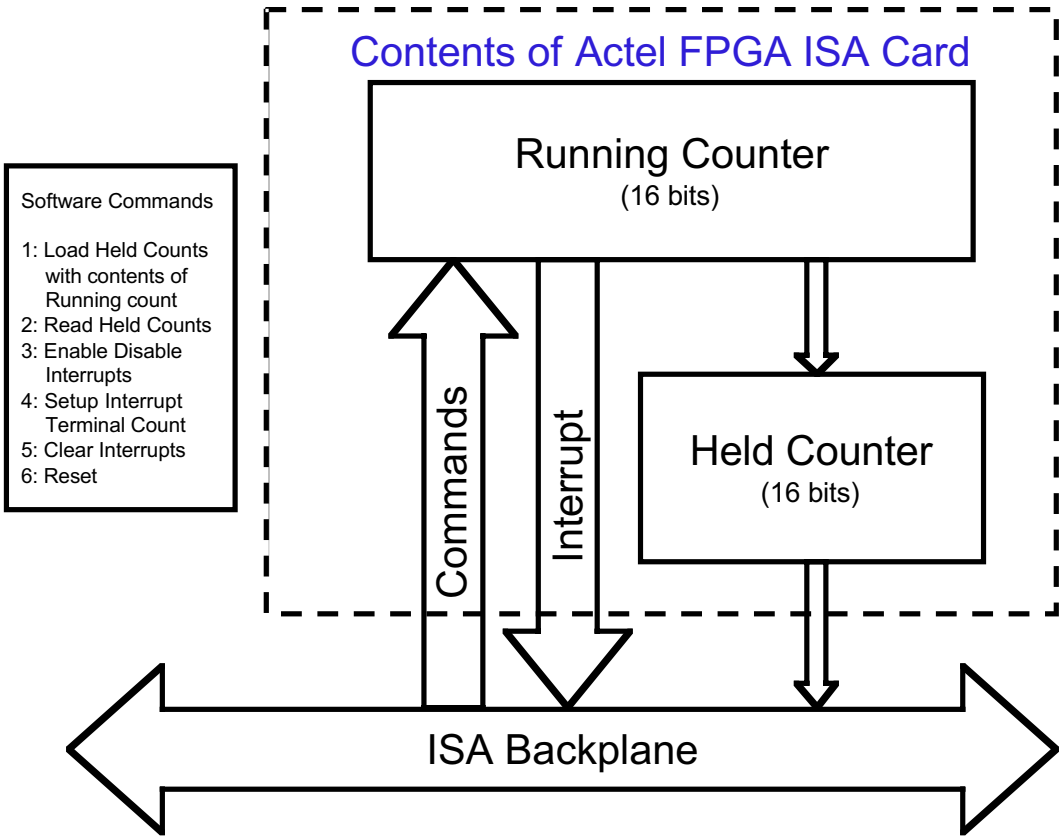

Figure 5. Photographs of Pentium III SC242 processor showing fan side and front side.

Intel Pentium III, Device Under Test (DUT)

The DUT processor is a modification of a standard Pentium III (P3) for the 242-contact slot connector (SC242, also called "Slot 1") module. (The P3 is available both in this form and in various 370-pin zero insertion force socket (PGA370) forms. The SC242 form was chosen for these tests for packaging/beam-access considerations).

An unmodified SC242 module, shown in Figure 6, has four discrete parts sandwiched and held together with single-use (they must be broken to be removed) spring clips. In order of arrangement from "back" side to "front" (or "fan") side they are a plastic backside cover, the printed circuit board (PCB) (See Figure 8, a picture of the DUT PCB without the other components), the heatsink, and a fan/front-side cover. The processor die is mounted active layer down onto an organic land grid array (OLGA), a small (1" x 1") PCB (with die mounted directly to it and substrate exposed), which is in turn mounted to the PCB. The PCB also carries power distribution and signal traces, high frequency and bulk power supply bypass capacitors and voltage identification jumpers. Level 2 cache memory (L2) is incorporated on-die for all P3 processors involved in this test (in some other versions of SC242 module processors L2 resides within plastic packaged ICs mounted to the PCB).

Figure 6. Photographs of Pentium III SC242 processor showing fan side and front side.

Each DUT processor module was disassembled and reassembled with the heatsink/fan assembly translated away from the card edge connector to improve irradiation evenness (the fins of the heatsink cause the depth of Al to vary substantially). A thermal transfer plate ("heat pipe") provided thermal conductivity from the DUT to the heatsink/fan assembly. No thermal pad material was used since electrical insulation was not required. Originally, 4 nylon screws were used to provide clamping force between the DUT PCB and the thermal transfer plate. That arrangement required very careful torquing of the screws to achieve even approximately the right mating force. A long-screw/spring/nut system was later developed for accurate force application. It also allows for easier removal and attachment of the thermal solution to the DUT PCB. Figure 7 is a picture of the modified DUT assembly showing the original mounting solution (nylon screws).

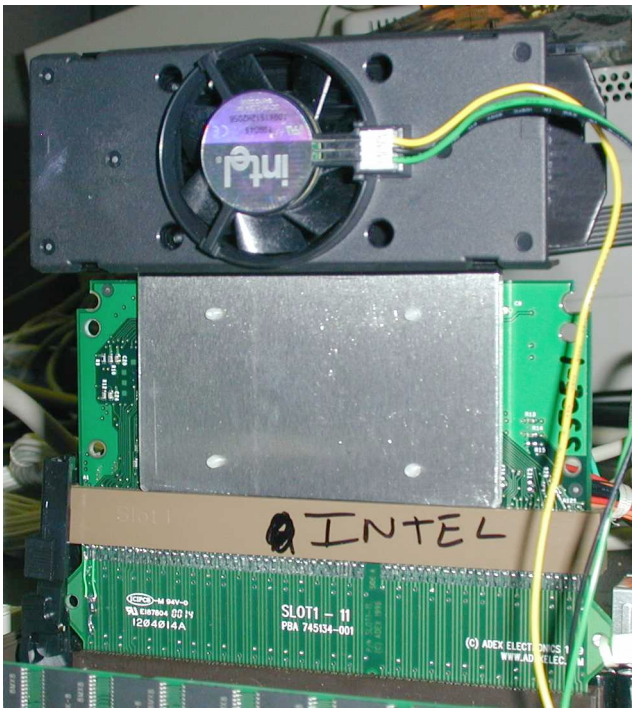

Figure 7. Beam-side view of the modified DUT. Visible sticking out of the Al thermal plate are the original white nylon attachment screws, later replaced with springs.

Of peripheral interest, the DUT cooling fans had a substantially higher failure rate than the DUTs themselves. Biased irradiation DUTs require the fan to be irradiated along with the DUT. Unbiased DUTs, originally, also had their fans and thermal transfer plates mounted, but after several fan failures it was found to be better to not irradiate the fans. Figure 9 shows electronics that reside within the fan cover. The unidentified IC with markings "6813 9772" is suspected. Later fans do not carry semiconductors with greater than three pins each. It is not known how sensitive these later devices are, and no quantitative data on the dose sensitivity of any of the fans was gathered.

Figure 8. The DUT PCB, showing the OLGA, and the epoxy fillet around the die.

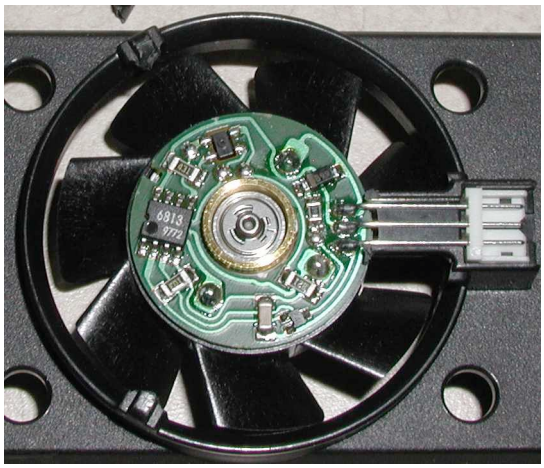

Figure 9. DUT fan with electronics cover removed, showing IC at left.

Signals that are controlled by the PXI subsystem or by the user from the user facility are:

Name	Destination	Description
PS_ON#	ATX Power supply	Hold low (0 V) for PS on; Open = High = Off
MotherPonoff	Motherboard power switch connector	Pulse low (0 V) to toggle power on and off
MotherSR	Motherboard reset switch connector	Pulse low (0 V) to initiate reset
Command &	COM1	RS-232 carrying commands to the

Telemetry		DUT subsystem (this also carries Telemetry to the PXI subsystem).
Keyboard	PS-2 keyboard port	

Signals that are monitored by the PXI or directly by the users in the user facility are:

Name	Source	Description
I_Vcc_core, Vcc_core	Extender board	Voltage samples of the core current and voltage. Twisted shielded pair (TSP): pair is both sides of the 1 mΩ current sampling resistance; shield is ground.
I_Vcc_L2, Vcc_L2	Extender board	Voltage samples of the DUT Level 2 cache current and voltage. TSP to both sides of the 10 mΩ current sampling resistance; shield is ground.
I_Vtt, Vtt	Extender board	Voltage samples of the DUT termination voltage source's current and voltage. TSP to both sides of the 10 mΩ current sampling resistance; shield is ground.
V_temp	Extender board	Voltage sample of the on-die temperature sensing diode. TSP.
Telemetry/ Command	COM1	RS-232 carrying telemetry from the DUT subsystem (this also carries Command information from the PXI subsystem).
Telemetry & OS output	VGA card	Video carrying telemetry, and OS/BIOS boot output to the user facility.

Test Software

The DUT software is compiled in Microsoft Visual C++ with a Pharlap Linker Add-in. The tests are written in a combination of C and assembly language. The software is executed using the Pharlap Real-Time Operating System. Pre-emptive task switching is turned off. The DUT communicates to the user through a VGA/keyboard interface and a serial port to the test controller system. All telemetry is echoed to a memory area that is not destroyed upon soft-reset or short power cycles. This memory is dumped through the serial port to the test controller after a reboot following a crash of the system. This is performed in an attempt to recover information lost due to the crash.

There are ten tests available for testing the Pentium III components. Each test sends a keep-alive at approximately a one hertz rate (0.1 Hz for test "H") and sends error results as they happen. One test is selected for each exposure to the beam and the software repeatedly performs the test until a pre-determined dose is reached or the software stops communicating to the user.

Test "A" checks the general-purpose registers of the CPU. There are eight general-purpose registers. Three registers are used by the program to keep track of execution parameters. The ESI register is used to point to a data area in memory where the values of the five registers under test are mirrored. The EAX register is used to keep track of the number of executions so that the keep-alive can be sent at proper intervals. The ESP register keeps track of the stack, which is used to store information when logging errors.

This test sets five CPU registers (EBX, ECX, EDX, EBP, and EDI) to a baseline value of 0AAAAAAAA Hex, then continuously checks to see if any of the register values change. If any values change, an error is reported to the user and an attempt is made to reset the register to its baseline value. The register is read again to form a new baseline value. The error report includes the following: the name of the register that changed,

the value it changed to, the baseline before the error and the baseline after the error. The test then continues. At each keep-alive the baselines are reset to 0AAAAAAAA Hex.

Test "B" checks the Floating Point Unit (FPU) with a maximum of data transfer to the FPU. A buffer is loaded with the arguments and expected results for the five operations tested (fadd, fsub, fmul, fdiv, and fsqrt). For each cycle through the test, the following sequence is followed for each operation: The first operand is transferred to the FPU from memory. The second operand is transferred to the FPU from memory. The operation is performed. The result is transferred to memory. The result is transferred back to the FPU and compared with the expected result. Any errors are saved to a log in memory and reported to the user at the next keep-alive. The EBX is used to keep track of the number of cycles run. When EBX passes a constant number of cycles a keep-alive is sent and any errors are reported.

Test C performs a memory test or cache test. If the cache is turned off, it performs a memory test otherwise, it performs a cache test. If the cache is on, then the cache is turned off, the memory is loaded with an incrementing pattern and the cache is turned back on before entering the test. The entire range is loaded with a baseline of 0AAAAAAAAH. The range is 131072 words for the memory test and the L1&L2 cache test and 8192 words for the L1 only test. The memory is checked word by word. After each word is checked, its value is changed to the bitwise complement of the baseline. If the value is not as expected then an error is reported and an attempt is made to reset the value to the baseline. The error report includes: the location address, the value read, the baseline and the value after attempting to reset to the baseline. If the value cannot be restored to the baseline, then checking is disabled for that location until the next keepalive. After the entire range is checked, the baseline is changed to its bitwise complement and checking starts again from the beginning.

Test "D" launches seven subthreads each with a counter that is reset to zero. Each thread increments its counter if the counter is less than 11 and then passes control to the next thread. The main thread then checks after 50 milliseconds to see if all of the counters have reached 11. If not an error is reported to the user. The test repeats continuously.

Test "E" runs through 16K of instructions repeatedly. The instruction sequence is to increment the eax register from 0 to 3 checking in between each increment to see if the value is as expected, then to decrement the eax register 3 times and check to make sure it returns to zero. Any errors are reported to the user and the cache is invalidated. Thirty of forty-six bytes in the code are continually used during proper execution; 65% of the 16K are exercised. The ECX register is used to keep track of the number of times the instructions are repeated. When ECX passes a constant number of cycles, a keep-alive is sent. The cache is flushed and the test is restarted whenever an error is detected.

Test "F" checks the Floating Point Unit (FPU) with a maximum of operations in the FPU. A buffer is loaded with the arguments and expected result. The operation tested is:

cos(cos(cos(sin(sin(sin(sqrt(sqrt(sqrt(sqrt(sqrt(sqrt(a*b))))))))))))

where a=0.123456789 and b=0.987654321. For each cycle through the test the following sequence is followed: The first operand is transferred to the FPU from memory. The second operand is transferred to the FPU from memory. The operations are performed. The result is transferred to memory. The result is transferred back to the FPU and compared with the expected result. Any errors are saved to a log in memory and reported to the user at the next keep-alive. The EBX is used to keep track of the number

of cycles run. When EBX passes a constant number of cycles a keep-alive is sent and any errors are reported.

Test "G" checks the Matrix Math Extensions (MMX). A buffer is loaded with the arguments and expected results for the four operations tested (pxor, por, pmul, pmulh, padds, addps, divps, and mulps). For each cycle through the test the following sequence is followed for each operation: The first operand is transferred to the FPU from memory (FPU registers are used by the Pentium for performing MMX functions). The second operand is transferred to the FPU from memory. The operation is performed. The result is transferred to memory. The result is compared with the expected result. Any errors are saved to a log in memory and reported to the user at the next keep-alive. The EBX is used to keep track of the number of cycles run. When EBX passes a constant number of cycles a keep-alive is sent and any errors are reported.

Test "H" measures the passage of time in CPU cycles against the ISA bus clock of 8.33MHZ. A timer board has been set up to provide an interrupt every 16383 cycles of the ISA bus clock. 5000 samples of the number of CPU cycles between interrupts are recorded and sent to the user after the test is complete in about 9.8 seconds. Then another test is started.

This test outputs a distribution of the number of CPU cycles between interrupts. The format of this output is as follows (each entry is in hex followed by a comma):

- the number of cycles for the first value in the list
- the number of samples below the lowest value in the list
- the number of samples beyond the highest value in the list
- the increment in number of cycles between entries in the list
- the list of values (comma separated) where a series of zeros is output as 0:v (v being the hex number of times to repeat the 0 entry). There is no comma after the last value in the list.
- The keep-alive: "H"

Test "L is used to verify that the CPU is still operating properly after changes in the setup or after a reboot. It loops through tests "A" through "H" repeating each test through two keepalives.

Test "N" is used in total dose testing. It continuously loops through tests "A" through "H" stopping every ten minutes for the test controller system to take voltage and current measurements. For these measurements, the test outputs "MEASURE <time>" to the telemetry signaling the test controller to take its measurements. It then waits 30 seconds for these measurements to be taken. Then it outputs "END" and continues looping through the tests until the next measurement time.

Test Methodology

Total Dose Test Process

To completely characterize the P3/K7 DUT for TID effects requires numerous parametric measurements, too numerous to measure without test equipment beyond the scope of this project. This level of characterization is not necessary for the needs of this project. To this end, it is sufficient to monitor the voltages and currents to the microprocessor, the instruction timing (to monitor the processor for timing critical operations), and microprocessor functionality.

This total ionizing dose response included exposure to protons and to Cobalt-60. Proton testing was carried out at the Indiana University Cyclotron Facility (IUCF) using 198 MeV protons incident on test structure with fluxes ranging from 10^6 to 10^9 protons/cm^2/sec. This proton TID testing was done in conjunction with the proton SEE testing. Cobalt-60 testing was done at the GSFC Radiation Effects Facility (REF) with dose rates ranging from 3 to 10 krads(Si)/day.

To accomplish the measurements mentioned above, the same test hardware that is used for SEE testing. For biased testing, the entire motherboard assembly is placed in the Cobalt chamber with all but the DUT heavily shielded. For unbiased testing, the DUT is placed in a test jig with grounded pins and removed from the chamber periodically into the full test setup for data collection.

Data collection consists firstly of the seven voltages and currents available through the extender card. Secondly, the DUT is fully exercised utilizing all the tests developed for SEE testing. Finally timing is monitored using a measurement of the access time of a data line and through the use of the Timer Card hardware and software.

Results

Intel P3 and AMD K7 parts were exposed to the total dose environment at the IUCF proton facility and the GSFC Radiation Effects Facility (Cobalt-60). The results of this testing are summarized in Table III for the P3 devices and Table IV for the K7 devices. It should be noted that the one DUT rated at 550 MHz is 0.25 μm technology, while all other DUTs tested are 0.18 μm technology.

TABLE IV
Pentium III DEVICE UNDER TEST (DUT) TABLE

Device	Rated Speed	Test Condition	Source	Exposure Levels (krads)
P3	800 MHz	Biased	Co-60	*511
P3	933 MHz	Biased	Co-60	573
P3	550 MHz	Unbiased	Co-60	336
P3	650 MHz	Unbiased	Co-60	336
P3	650 MHz	Unbiased	Co-60	3700
P3	700 MHz	Unbiased	Co-60	336
P3	850 MHz	Unbiased	Co-60	697
P3	933 MHz	Unbiased	Co-60	2100
P3	550 MHz	Biased	Protons	4.9
P3	650 MHz	Biased	Protons	52
P3	650 MHz	Biased	Protons	4.4
P3	700 MHz	Biased	Protons	100
P3	700 MHz	Biased	Protons	5.5
P3	700 MHz	Biased	Protons	8.9
P3	750 MHz	Biased	Protons	14.3
P3	850 MHz	Biased	Protons	0.3
P3	850 MHz	Biased	Protons	13.3
P3	850 MHz	Biased	Protons	47.5
P3	933 MHz	Biased	Protons	16.9
P3	933 MHz	Biased	Protons	46.7
P3	933 MHz	Biased	Protons	34.4
P3	1 GHz	Biased	Protons	45.3
P3	1 GHz	Biased	Protons	32.5
P3	650 MHz	Unbiased	Protons	26

** Functional Failure Dose.*

The parts tested at IUCF were exposed to protons in unbiased and biased states and exposed to proton doses ranging to approximately 100 krads(Si) with various increments. After each dose point, the all parts passed all functional tests and the monitored voltages and currents did not change. No parametric timing measurements were done in these tests. These tests are expected to be the most sensitive to dose. The parts, however, did not degrade in timing sufficiently to fail any of the functional tests that were performed.

Total dose testing using the Cobalt-60 source at GSFC was stopped on 3/8/02, due to the GSFC Facility shutting down for maintenance. Several P3 devices, in an unbiased

condition, have been exposed to various doses, one in excess of 3700 krads(Si). They have shown little sign of degradation in either supply currents or timing and functionality testing. Biased testing of one Pentium III DUT did functionally fail after exposure to an approximate dose of 511 krads(Si). A replacement part was tested under bias, and had exceeded a dose of 573 krads(Si) when it was finally removed.

TABLE IV
AMD K7 DEVICE UNDER TEST (DUT) TABLE

Device	Rated Speed	Test Condition	Source	Exposure Levels (krads)
K7	600 MHz	Biased	Protons	4.4
K7	650 MHz	Biased	Protons	3.6
K7	700 MHz	Biased	Protons	0.5
K7	900 MHz	Biased	Protons	7.2
K7	1 GHz	Biased	Protons	3.2
K7	1 GHz	Biased	Protons	0.1
K7	650 MHz	Unbiased	Protons	100

There were plans to expose the AMD K7 processors, both biased and unbiased, to Cobalt-60. However, after the poor showing the parts made at the heavy ion facility (see next section), it was determined to remove the AMD K7 parts from this study.

This proton total dose testing seems to indicate that these generations of AMD K7 processors are TID hard to greater than 100 krad(Si), based on minimal test data. However, based on substantial data collected via proton and Cobalt-60 exposure, the Intel Pentium III processors are extremely tolerant to total dose, with unbiased parts surviving in excess of 3.7 Mrads(Si) and biased parts surviving in excess of 500 krads(Si).