

National Aeronautics and Space Administration



# Analog Devices AD7847SQ/883B 12-bit MDAC Single-Event Latchup Characterization Report

Test Date: 05 December 2010  
Today's Date: 15 December 2010

Plan Date: 15 November 2010

Principal Investigator(s): Jonathan Pellish and Raymond Ladbury  
Test Engineer(s): Alvin Boutte  
Project: Global Precipitation Measurement (GPM) mission



## 1. Reference Documents

- Kinoshita, G.; Kleiner, C.T.; Johnson, E.D.; , "Radiation Induced Regeneration through the P-N Junction Isolation in Monolithic I/C's," *IEEE Trans. Nucl. Sci.*, vol.12, no.5, pp. 83-90, Oct. 1965.
- Johnston, A.H.; , "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Trans. Nucl. Sci.*, vol.43, no.2, pp. 505-521, Apr 1996.
- Hutson, J.M.; Pellish, J.A.; Tipton, A.D.; Boselli, G.; Xapsos, M.A.; Kim, H.; Friendlich, M.; Campola, M.; Seidleck, S.; LaBel, K.; Marshall, A.; Deng, X.; Baumann, R.; Reed, R.A.; Schrimpf, R.D.; Weller, R.A.; Massengill, L.W.; , "Evidence for Lateral Angle Effect on Single-Event Latchup in 65 nm SRAMs," *IEEE Trans. Nucl. Sci.*, vol.56, no.1, pp. 208-213, Feb. 2009.
- "IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-Circuit Process Characterization," *IEEE Std 1181-1991*. (Deprecated)
- JEDEC JESD57

## 2. Purpose

The purpose of this testing was to characterize the Analog Devices AD7847 multiplying digital-to-analog converter (MDAC) for single-event latchup (SEL) susceptibility. These data will be used for flight lot qualification purposes.

## 3. Test Samples

Three (3) parts were being provided for SEL testing. A minimum of two devices will be exposed to heavy ion irradiation. More information about the devices can be found in Table 1.

The parts were prepared for testing by removing the glass-sealed ceramic lid from the target die. The parts were fabricated in BiCMOS technology. Since we do not know the number of overlayers used in these processes, linear energy transfer calculations were recorded based on the top-surface incident ion species and kinetic energy, and we ensured that the particles had a range in Si of more than 100 microns from the top of the die.

**Table 1: Part Identification Information**

Qty	Part Number	LDC	Source	Package
3	AD7847SQ/883B 5962-9451802MLA	0801A	Analog Devices	CDIP4-T24

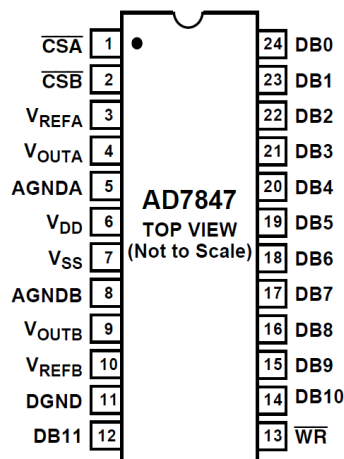


Figure 1: Pin diagram for AD7847 MDAC

## 4. Test Facility

**Facility:** Texas A&M University Radiation Effects Facility. Tune: 15 MeV/amu

**Flux:**  $5 \times 10^3$  to  $5 \times 10^5$  ions  $\text{cm}^{-2} \text{s}^{-1}$

**Fluence:** All tests will be run to a fluence of  $1 \times 10^7$   $\text{cm}^{-2}$  or until a latchup event is observed

Table II: Ions Used for Device Irradiation (in priority order)

Ion	Energy (MeV)	Range in Silicon	Silicon LET (MeV $\text{cm}^2/\text{mg}$ )
<sup>197</sup> Au	2247	118	85.4
<sup>109</sup> Ag	1170	107	44
<sup>40</sup> Ar	508	180	9

Note that energy, range, and LET are calculated based on 1 mil aramica window and 50 mm of air prior to the silicon target. When we arrived at the facility, Au was available and tuned, so the decision was made to go with this ion. Because we were unable to observe SEUs SETs or other single-event effects, failure to observe SEL at this highest LET (sufficient to qualify the device even at normal incidence) obviated the need to test with lower LET ions.

## 5. Test Conditions and Error Modes

AD7847SQ	
Test Temperature	80° C
Operating Frequency	150 kHz
Power Supply Voltage	+/- 15 Vdc
Parameters of Interest	LET <sub>th</sub> , temperature, supply voltage
SEE Conditions	Prolonged and self-sustained high-current state

Current limit was set to 110% of absolute maximum rating. In the event of observing SEL, a destructive test limiting current to 1 A could be run.

## 6. Test Methods

The test circuits for all three devices were built to approximate the intended application. The accompanying figure captures the essentials of the application.

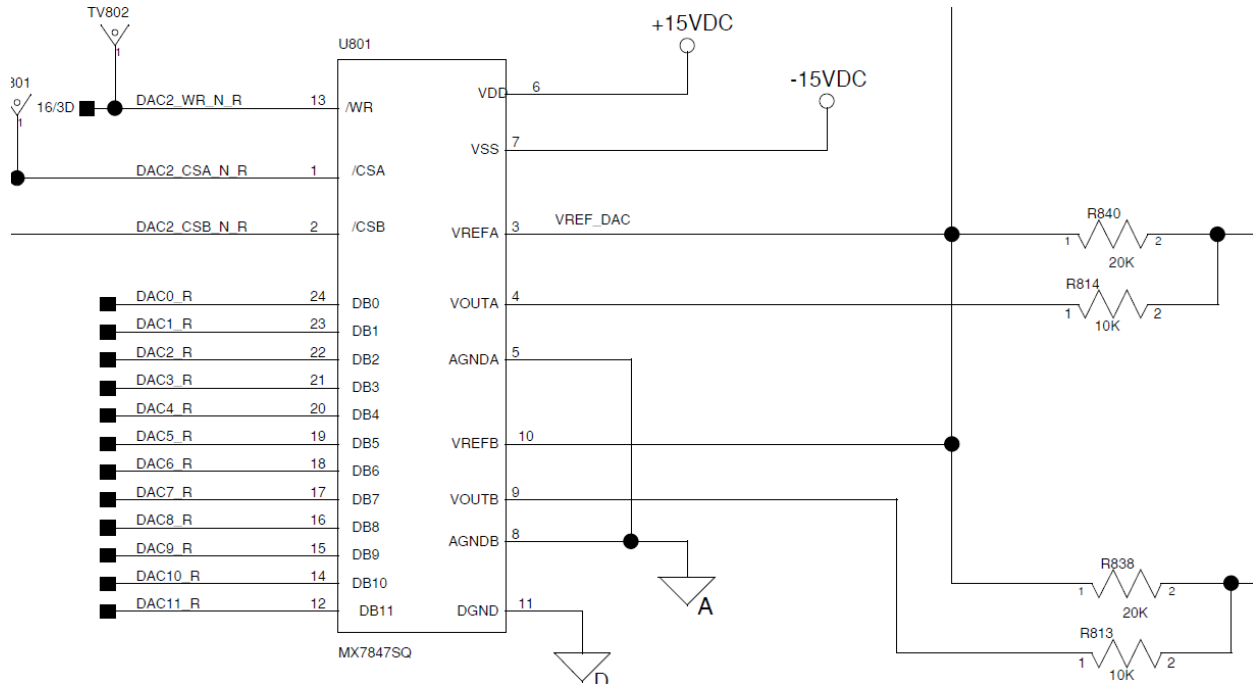


Figure 2 Application circuit upon which test circuit was based.

Application-specific circuits are shown on the last page of this document and in an external PDF file. Voltages on I/O will be assigned as necessary. The digital outputs were left floating. Vdd and Vss were +15 and -15 V respectively. The digital inputs were tied low. WR\_BAR was toggled at the application frequency to simulate latching data into the input registers, and CSA\_BAR and CSB\_BAR were tied low to enable data latch into each DAC's input register.

The test setup required only power supplies and data logging equipment. The power supplies were located in the irradiation cave, while the data logging equipment was in the control. Each test board had a single device under test, with new samples switched by hand.

## 7. Test Performance

Test personnel included Alvin Boutte and Ray Ladbury. Eight hours were allotted for the test. A test would be stopped if an SEL were seen or if the effective fluence reached  $1 \times 10^7$  ions/cm<sup>2</sup>. The following table is a rough outline of the tests planned during the test slot.

Table III: Test Condition Plan

Condition	Temp (°C)	Tilt (°)	Roll (°)	Ion	Notes
1	80	0	0	Au	Worst-case, normal incidence
2	80	45	0	Au	Repeat first condition at steeper angle
3	80	60	90	Au	Roll part orthogonal to the beam at the same tilt angle for even coverage in the 1 <sup>st</sup> octant
4	80	0	0	Au	Locate <u>threshold voltage</u> for SEL at normal incidence. Only necessary if SEL observed.
5	SEL <sub>th</sub>	0	0	Au	Locate <u>threshold temperature</u> for SEL at normal incidence. Only necessary if SEL observed.
6	80	0	0	Ag	Repeat tantalum conditions with silver; 1–3. Cond. 4 & 5 only necessary if SEL is observed.
7	80	0	0	Ar	Repeat tantalum/silver conditions with argon; 1–3. Cond. 4 & 5 only necessary if SEL is observed.

## 8. Results

No evidence of SEL or other prolonged/sustained current anomalies was seen for Au incident at either normally or a 45° to the normal (tilt or roll) and for worst case conditions of 80 °C and supply voltages +/-15 V. This obviated the need to test with lower LET ions. We also note that the normally incident LET of 85.4 MeV•cm<sup>2</sup>/mg is sufficient to qualify the device, so that consideration of range at angle is unnecessary.

## 9. Conclusion

Although no SEL was seen for the worst-case application conditions, this test did not measure susceptibility of the AD7847 to nondestructive SEE. If these are a significant concern in future applications, additional testing will be needed to characterize susceptibility to these threats.

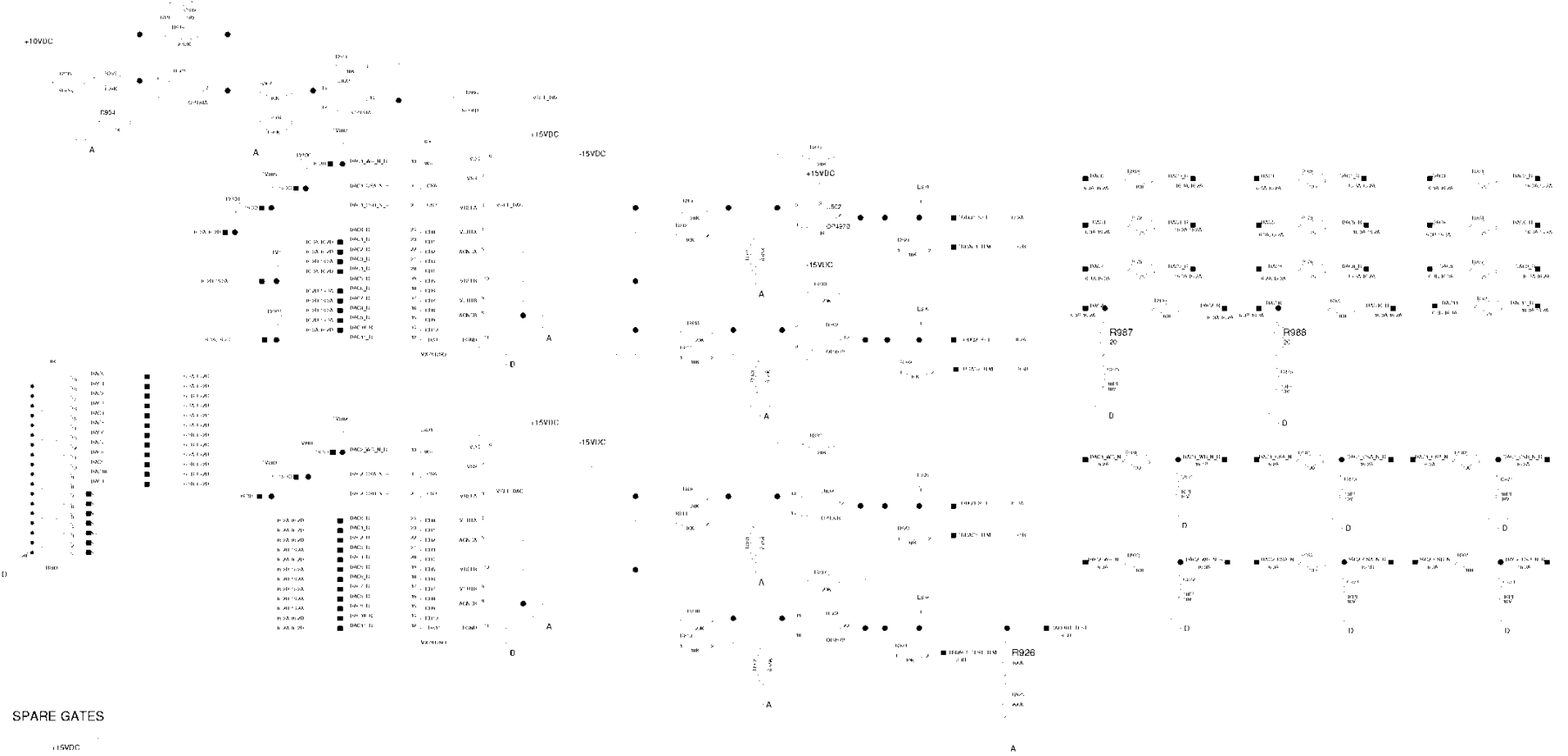
## 10. URLs for Device Data Sheets

- AD7847SQ/883B
  - Generic part
    - [http://www.analog.com/static/imported-files/data\\_sheets/AD7837\\_7847.pdf](http://www.analog.com/static/imported-files/data_sheets/AD7837_7847.pdf)

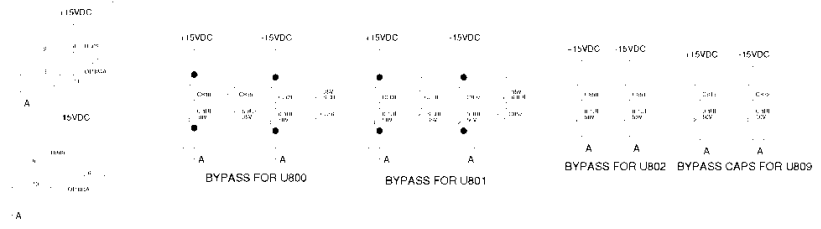
- PCNs
  - [http://www.analog.com/static/imported-files/PCN/ADI\\_PCN\\_04\\_0080\\_Rev\\_1\\_Form.pdf](http://www.analog.com/static/imported-files/PCN/ADI_PCN_04_0080_Rev_1_Form.pdf)
- DSCC part
  - <http://www.dscclia.mil/Downloads/MilSpec/Smd/94518.pdf>

# Appendix for Schematic Diagram

## DAC FOR TORQUER BAR DRIVE CIRCUITS



### SPARE GATES



Place close to U800 for terminate case

Place close to U801 for terminate case

MACE-A7B MODULE ELECTRICAL SCHEMATIC	
DATE	11/19/88
BY	GD
NO.	2117060
REV.	10/20