LTC1864L Single Event Effects (SEE) Test Report

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1. INTRODUCTION

This study was undertaken to determine the single event destructive and transient susceptibility of the LTC1864L Analog to Digital Converter (ADC). The LTC1864L is referred to as the "Device Under Test" (DUT). The DUTs were monitored for Single Event Latch-up (SEL) and Single Event Upset (SEU) induced faults by exposing them to a heavy ion beam.

2. BACKGROUND

ADCs are widely utilized in critical space applications. As a part of the device selection process, it is essential to perform error-rate calculations to determine if the device will satisfy system requirements while operating in harsh radiation environments. Error rate calculations for such environments are based on the device's Single Event Effects (SEE) characterization and associated SEE cross-sections. SEE cross-sections are generally calculated by counting error events as the devices under test (DUTs) are irradiated. Parameters used in SEE rate calculations are the number of error events per particle fluence, linear energy transfer (LET) of particles, and the targeted environment.

Original approaches to ADC SEE testing have been based on manufacturer type parametric testing. Variations to these tests are being implemented in order to satisfy SEE evaluation. It is important to note that parametric testing is the process of characterizing ADC intrinsic noise. However, upsets categorized as SEEs are due to particle ionization and their error signatures are starkly different than intrinsic noise. It follows that a different testing methodology from parametric testing is required for SEE analysis.

In response, the NASA Radiation Effects and Analysis Group (REAG) is developing and evaluating novel approaches to SEE test strategies for various types of ADCs.

ADC devices can be categorized by architecture type: Serial or Parallel. The two architectures differ in sampling schemes, conversion process, operational speeds, and I/O interfaces. The LTC1864 falls into the serial ADC category.

2.1 Parametric Testing versus SEE Testing

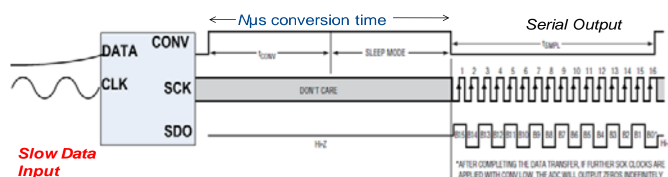

Figure 1: Serial ADC I/O Interface. Digital output timing waveforms are included. DATA: analog data input signal, CLK: reference CLK, CONV: conversion indicator (also known as STROBE), SCK: output CLK for serial output data, SDO: serial data output stream.

Serial ADC devices are generally used to monitor relatively slow changing analog signals such as temperature, voltage, pulse-width-modulator motor control, etc…. As illustrated in Figure 1, modern serial ADCs have a conversion process in the µs range and limit input data frequencies to the KHz range. The digital output interface is serial and hence takes several clock cycles to receive the full converted digital code word.

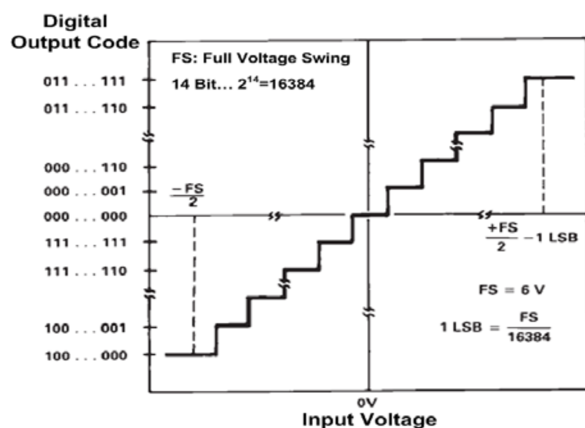

Figure 2: ENOB code word quantization. All 2^N code words are evaluated

Serial ADC parametric testing includes evaluating code word offsets from expected values. Offsets are characterized by the Effective Number of Bits (ENOB) and will manifest in the lower order code word bits. For an N-bit code word, parametric testing sweeps through all 2^N codes for worse case analysis as illustrated in Figure 2.

The difference in SEE analysis versus parametric characterization is that most of the SEE upsets are in the form of various size transients in the analog circuitry that can be captured into the digital domain. Other types of SEEs can cause digital logic to flip their states. Consequently, serial ADC error signatures are not limited to the lower order bits as with ENOB. In addition, SEE analysis encompasses a wider range of parameters and considerations:

Statistical analysis requires multiple upsets to be captured and evaluated

Various types of upsets can occur due to affected circuitry. This includes code word upsets and control circuitry malfunction. Such events are not a portion of parametric testing.

Small differences in input voltage generally do not affect SEE error signatures. As an example, an input voltage that outputs a code word=1000 decimal will have a statistically equivalent upset rate as input voltages that produce code words near 1000 decimal.

Due to financial and time constraints, the number of radiation tests is limited.

The question then becomes, if all 2^N code words cannot be fully evaluated during radiation testing, will a subset suffice? It has been observed that testing at least three code words provides a sufficient set of SEE test data. If the minimal set is selected for testing, the code words should be associated with input voltages at the upper and lower extremes of the device including the center voltage. However, if time and money allow, it is always recommended to evaluate as many code words as possible.

3. DEVICES TESTED

3 DUTs were tested.

3.1 Part Number and Codes

The full part number is LTC1864LAIMS8HPBF
LTC7E3
9D17 (lot/date code)

3.2 LT1864L Datasheet Characteristics

Figure 3: LTC1864L Schematic

Device Features as listed in the LT1864L Datasheet

- 16-bit 150ksps ADC in MSOP Package
- Single 3V Supply
- Low Supply current: 450uA(Typ)
- Auto Shutdown Reduces Supply current to 10uA at 1ksps
- Differential inputs
- SPI/MICROWIRE Compatible Serial I/O
- No Minimum Data transfer rate

3.3 LTC1864L Interface to Tester

Table 1: LTC1864L I/O with respect to DUT

I/O Name	Width	Dir wrt to DUT	Description
SCK	1	OUT	Shift Clock Input. This clock synchronizes the serial data transfer
SDO	1	OUT	Digital Data Output. The A/D conversion result is shifted out of this pin
CONV	1	OUT	Convert input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is

			finished, the part powers down. A logic low on this pin enables the SDO pin and allows converted data to be serially shifted out.
DATA_CH0	1	IN	Analog Data input (IN+)
DATA_CH1	1	IN	Analog Data input (IN-)

4. LTC1864 TEST METHODOLOGY

While testing ADC devices, it is important to minimize noise due to test setup. Currently the test setup illustrated in Figure 4 has proven to inject the lowest noise into the system. After the test environment noise is characterized, expected code words are calculated based on the predetermined set of input stimulus.

During irradiation, input stimulus is supplied by the signal generator to the ADC and code words are compared to their expected values to determine when SEEs occur. Because transients can also affect ADC control circuitry, tests should monitor if the ADC is not responding to the stimulus such that the conversion process is inoperable.

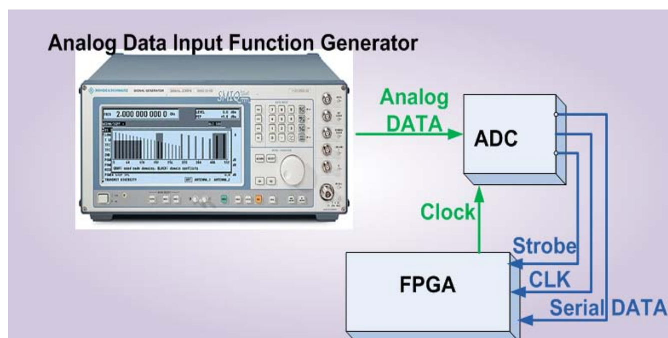

Figure 4: Serial ADC test setup

Two testing methodologies were performed: Single Point (SP) and Differencing (DP).

4.1 LTC1864 Single Point Testing Scheme

The single point SEE test methodology requires the analog data input to be a static value. The following is the SP algorithm.

- Set parameters for SP testing (turn on and off Sleep mode, and error bounding window size is set).
- Set the analog function generator to a constant value.
- Turn the LCDT tester on via LAB view test command
- Expected values are calculated (no beam):
- LCDT toggles conversion pin
- LCDT captures ADC output values (serial capture)
- Expected value is calculated as average value of 1024 ADC output codes
- LCDT automatically exits expected value calculation mode and is ready to process SEE data
- Heavy Ion Beam is turned on

LCDT compares sampled input data to expected value previously captured. If input data falls outside of *expected±error bound,* then an upset message is sent to the tester

4.2 LTC1864 Differencing Testing Scheme

The DP SEE test methodology requires the analog data input to slowly change its value. The function generator is set as a 10HZ ramp function.

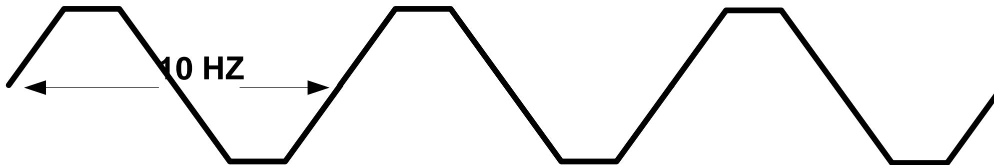

Figure 5: Functional Generator Ramp Function used for DP method

The following is the DP algorithm.

- Set parameters for DP testing (turn on and off Sleep mode, and differencing window size is set).
- Set the analog function generator to a ramp Function.
- Turn the LCDT tester on via LAB view test command
- Heavy Ion Beam is turned on
- LCDT compares current sampled input data to last sampled value that was previously captured. The difference should fall into the differencing window. If difference falls outside of *window,* then an upset message is sent to the tester

4.3 Test Methodology trade offs

The DP method enables testing across a wide range of input voltage (and hence code word) values. However, it requires a larger error window (differencing window) than the SP method. Consequently, the SP method proves to be a more efficient means for analyzing upsets that cause small variations in the LSB of the codeword.

5. LOW COST DIGITAL TESTER (LCDT) TEST VEHICLE

The following sections describe the construction of the Low Cost Digital Tester (LCDT) including communication interfaces with the DUT and user PC. Figure 6 is a picture taken at the Texas A&M Heavy Ion Cyclotron Facility illustrating the LCDT connected to the DUT ready to be irradiated.

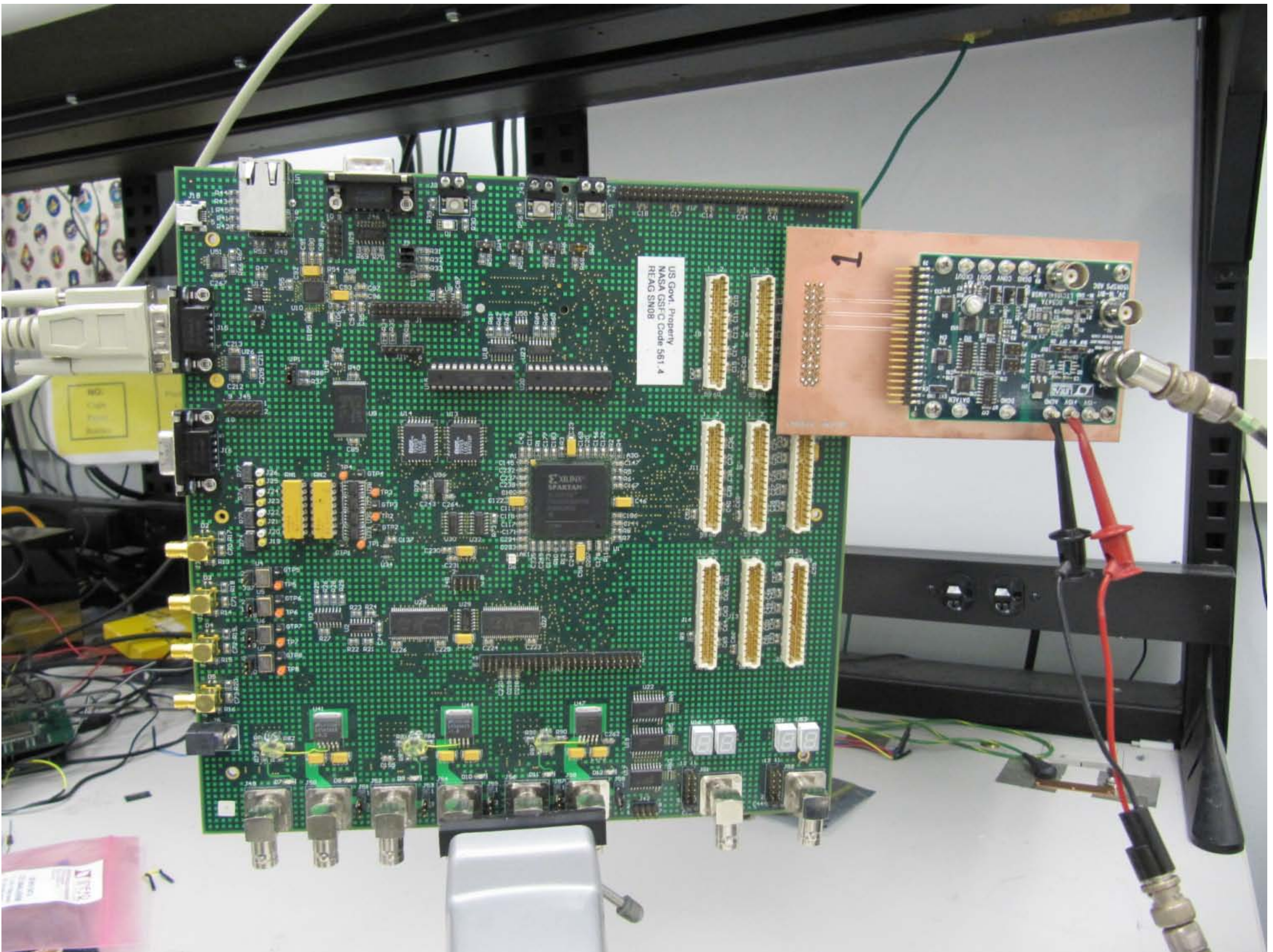

Figure 6: Picture of Low Cost Digital Tester (LCDT) connected to Device Under Test (DUT) at Texas A&M Heavy Ion Facility

5.1 Test Vehicle Architectural Overview

The LTC1864L controller/processor is instantiated as a sub component within the LCDT. The test set-up consists of a Mother Board (FPGA Based Controller/Processor) and a daughter board (containing DUT and its associated necessary circuitry). The LCDT communicates with a user controlled PC. The user interface on the PC is LAB-VIEW. The user is able to send commands via LAB VIEW to the LCDT and receive information from the LCDT. Please see Documents: “LCDT” and “General Tester” for further information concerning the LCDT functionality. The test setup is shown in Figure 6.

The objective of the DUT Controller/processor (in the LCDT) is to capture the converted ADC (digital) data and process the data to determine if an SEU occurred. In order to minimize LCDT to PC data transfer, only information pertaining to SEUs are sent to the PC (i.e. only data samples that are considered in error are sent to the PC).

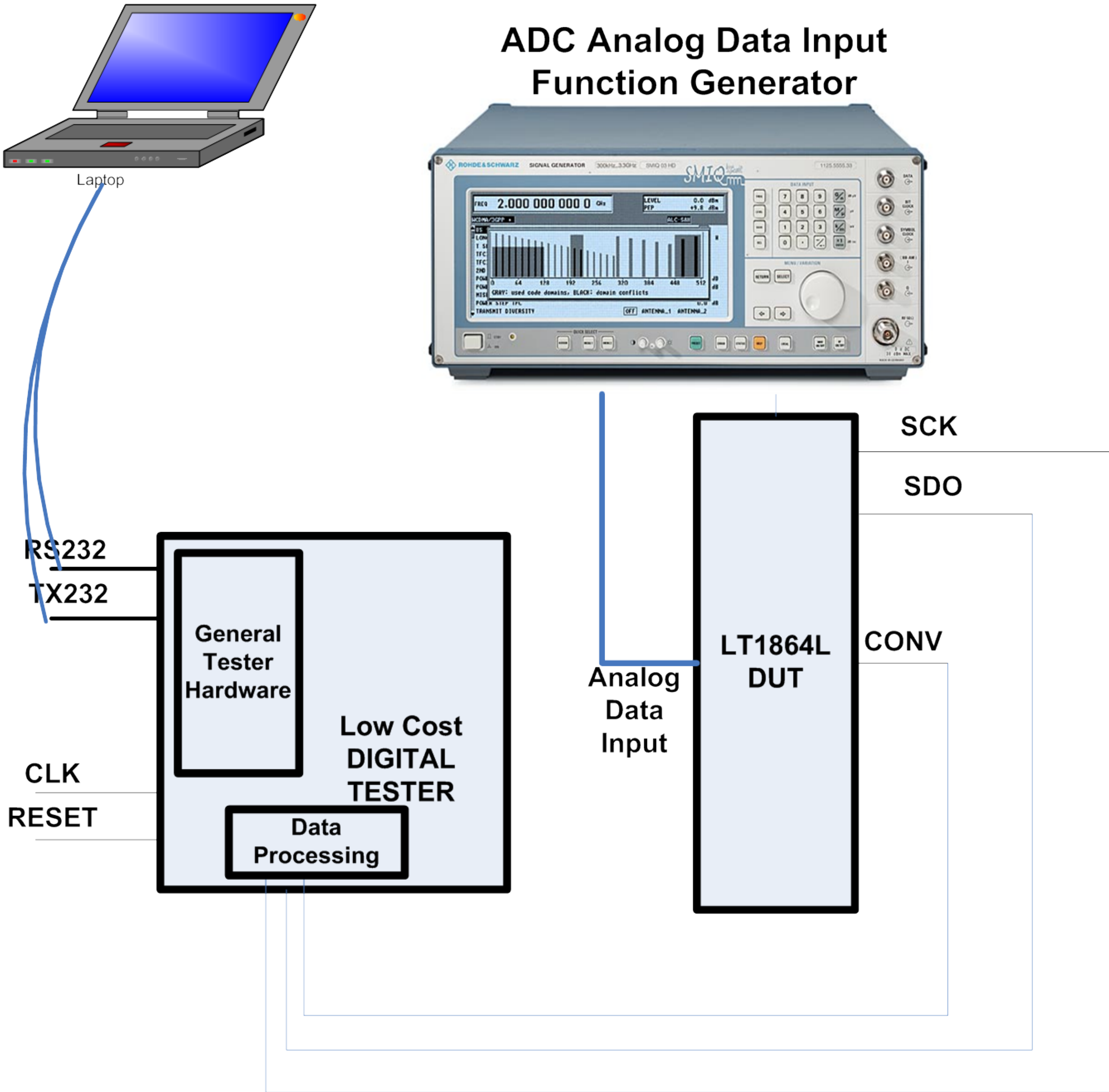

Figure 7: System Level Tester Architecture. One PC is running a Labview GUI. The PC sends commands to the LCDT to set test parameters and start test operations. The function generator provides ADC data input. Single Point (SP), the signal generator is set to a constant value. Differencing Points (DP), the signal generator sweeps through the entire range of points.

5.1.1 I/O List and Definitions

Interface tables were supplied in the previous sections for all of the designs.

Table 2: I/O for LTC1864L LCDT.

Input Name	bits	Direction Wrt to LCDT	Description
CLK	1	IN	System clock of the LCDT from Board crystal
RESET	1	IN	LCDT system reset from Power supply
RX232	1	IN	Serial receive input from Host PC. Used for PC to send commands to the LCDT
TX232	1	OUT	Serial transmission line to Host PC. Used to Echo commands and to send back either Shift Register or Counter Error Data
SCK	1	IN	Shift Clock Input. This clock synchronizes the serial data transfer
SDO	1	IN	Digital Data Output. The A/D conversion result is shifted out of this pin
CONV	1	out	Convert input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this pin enables the SDO pin and allows converted data to be serially shifted out.

5.2 RS232 communication from the LCDT to the Host PC

All RS232 communication from the LCDT to the host PC is prefaced with a header. . Information from the LCDT to the Host PC is one of the following listed in Table 3: an alive-timer, a command echo, or an Error Record.

Table 3: A list of the LCDT to Host PC RS232 Header bytes. Only the LCDT uses header information. The host PC sends pure commands to the LCDT without headers.

Header	Description

00 FA F3 20 — Alive Header No data bytes follow (i.e. only the header is sent from the LCDT to the PC)

00 FA F3 22 — Command Echo. 4 data bytes follow that represent the command that was previously sent from the Host PC to the LCDT.

00 FA F3 21 — Data Error Record: 23 bytes follow.

5.3 RS232 communication From the Host PC to the LCDT

Communication from the host PC to the LCDT does not contain a header. Information sent from the host PC to the LCDT are commands and are all 4 bytes in length The interface is controlled by a user GUI designed with LabView software.

5.3.1 User GUI

Commands are sent by typing specific values into Labview fields or controlling Labview on/off buttons listed on the screen.

The following section describes the commands sent from the Host PC to the LCDT.

5.3.2 User Interface and Command Control

The User controls the tests via a LABVIEW interface running on a PC. The PC communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word.

Table 4 : Summary of Commands Used in PROASIC Tester

Command #	Command	D0	D1	D2	Description
01	Reset LCDT	x	x	x	Resets the tester
02	Test Enable	x	x	x	Starts convert/capture ADC process. For SP, the initial phase is to calculate expected value by capturing 1024 ADC input codewords and taking an average.
90	Test Select	D	x	x	SP or DP selection. Default is SP. (D1 D0)=00 selects SP (D1 D0)=10 selects DP

B0	Error Window	D	D	x	SP:Window used with expected value for data compare. (code word must be this specified distance from the calculated expected value) DP: maximum difference between two consecutive captured code words
B1	Bin Range	D	D	D	Set to 10% of input voltage range. 3 bins are set around the max, average, and min input voltages. Code words are flagged if they fall into a bin. Flags are not errors – flags are only used as additional information in order to analyze upsets.
B2	Number of points per analog input cycle	D	D	D	DP only. Number of sample points required to complete one data input cycle. Example: 10Hz data input B2 00 30 d4 (12500 pts per cycle)
B3	Time Window	D	D	D	DP only. Roughly 2% of number of points per cycle. Used to determine if code word is moving at the correct rate of change Example: B2 00 30 d4 B3 00 00 FA (250 decimal)
B4	Sleeptime	D	D	D	Number of Clock Cycles (100MHz) that CONV pin stays active after actual ADC conversion time. Any excess time that CONV stays active places the ADC in sleep mode (see datasheet for more information)
C2	Data dump	x	x	x	Debug command. LCDT sends all samples to tester. Once the internal FIFO overflows some

					data items will be lost
7D	Print Sample	x	x	x	Debug command. LCDT sends current sample to tester

6. DUT TEST PROCEDURES

6.1 Test Objectives

The objectives of testing are to determine:

- Device upset rates
- Sleep-time effects
- Voltage data input effects

6.1.1 Running an SP Test

1. Bias the DUT (turn on power)
2. Set error window. (B0 D D X)
3. Set Sleep time (B4 D D D)
4. Send Start test command (02 xx xx xx)
5. First milliseconds, the DUT automatically calculates an expected value by capturing 1024 data points (output code words) and then taking the average.
6. Tester automatically places itself in test mode after calculating expected values. Test mode compares the DUT output code word to the expected value.
7. User monitors the output to ensure that there are no errors in test mode before the beam is turned on.
8. If errors exist when there is no beam, then user should check test setup or slightly increase error window
9. Turn on Beam (irradiate DUT)
10. While beam is turned on, the tester captures DUT code words and compares to expected value
    - If error during read, then the LCDT records that an error has occurred and sends the data value with timestamp to the PC
    - Goto 4 if not done with test else goto 6
11. Stop Beam
12. Reset Tester and DUT to prepare for next test

6.1.2 Running a DP Test

13. Bias the DUT (turn on power)
14. Set error window. (B0 D D X)
15. Set Bin Size (B1 D D D)
16. Set number of points per data input cycle (B2 D D D)
17. Set Time window (B3 D D D)
18. Set Sleep time (B4 D D D)
19. Send Start test command (02 xx xx xx)
20. First milliseconds, the DUT automatically calculates an expected value by capturing 1024 data points (output code words) and then taking the average.

21. Tester automatically places itself in test mode after calculating expected values. Test mode compares the DUT output code word to the expected value.
22. User monitors the output to ensure that there are no errors in test mode before the beam is turned on.
23. If errors exist when there is no beam, then user should check test setup or slightly increase error window
24. Turn on Beam (irradiate DUT)
25. While beam is turned on, the tester captures DUT code words, take difference from previous codeword, and compares to expected value
    - If error during read, then the LCDT records that an error has occurred and sends the data value with timestamp to the PC
    - Goto 4 if not done with test else goto 6
26. Stop Beam
27. Reset Tester and DUT to prepare for next test

7. PROCESSING THE DUT OUTPUTS

The outputs of the DUT are fed to the tester for data processing. The objective of the data processing is to capture data from the DUT, compare to an expected value, and report to the host PC if there is an error. The DUT system clock and reset signals are generated in the LCDT.

7.1 SP Data Processing

The tester compares the incoming codeword to its expected value using equation (1).

Xsample: DUT codeword (current sample)

E: Expected value

Errorbound: user defined window (samples are not expected to be strictly equivalent to the expected value due to noise within the device and test setup)

(1)

If the sample falls outside of the errorbound window from the expected value, an error is flaged, an error record is formed, and then the record is sent to the host PC via an RS232 link.

7.2 SP Error Record

Table 5 SP Field Table

Field	Field	Description
Data Pattern	15…0	Sample code word from DUT
Error Flag	79…64	Expected value (calculated by tester during startup)
Error Count	143…128	Current error counter from tester (does not filter bursts)
Debug	144	Flag indicating if record is debug information (user driven by command C2 or 7D)
Time Stamp	175…152	Cycle counter. Must multiply by the DUT frequency to convert to time. Used to determine error burst sequences

7.3 DP Data Processing

DP testing requires an input that sweeps across a large range of analog inputs as illustrated in Figure 5 and Figure 8. When calculating the difference between samples, information pertaining to the current sample and error can be lost. As an example, if the device stops working and outputs a constant or fluctuates around some value when not expected, performing a difference will not indicate an error because the distance function will always be satisfied. Consequently, there are a variety of conditions that are monitored that are based on the current sample:

1. Difference between samples
2. Is the current value out of range (greater than the maximum expected codeword or less than the minimum expected codeword)
3. Do the codewords sweep the full range within a specified time. This monitor indicates whether the output code words are stuck fluctuating around some value.

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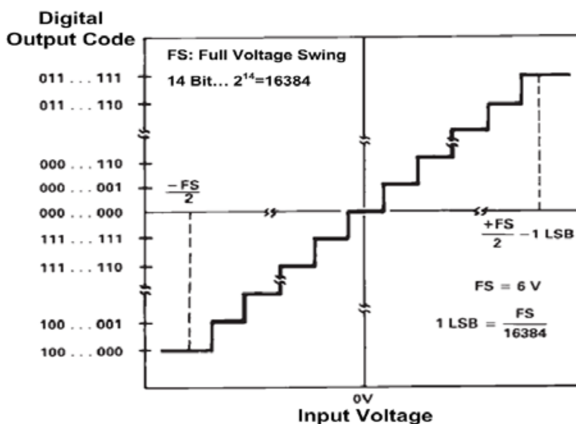

Figure 8: Input voltage range comparison to output code-words.

7.3.1 Difference Calculations

The tester compares the current codeword sample to the previous codeword sample using equation (2).

Curr_sample:	DUT codeword (current sample)
Prev_sample:	DUT codeword previous sample
Difference:	Maximum distance between codewords. Set by user

(2)

If the distance of the current sample from the previous sample is greater than the user specified value (difference), an error is flaged, an error record is formed, and then the record is sent to the host PC via an RS232 link.

7.3.2 Out of Range calculations

Prior to testing and upon a reset, the tester will monitor the input codewords for 100's of cycles to determine the maximum codeword and minimum codeword reached. The average maximum codeword is calculated by the tester and the average minimum codeword is calculated by the tester. The averages are used as boundaries during the out of range test. The sample must satisfy Equation (3) to not be considered an error.

Curr_sample: DUT codeword (current sample)

AverageMIn: Tester calculated minimum codeword boundary. Codeword must be greater than this value or an error is reported

AverageMax: Tester calculated maximum codeword boundary. Codeword must be less than this value or an error is reported

(3)

7.3.3 Codeword stuck-at monitors

Prior to testing and upon a reset, the tester will monitor the input codewords for 100's of cycles to determine the average number of cycles it takes for the codewords to reach minimum and maximum values. During irradiation, the tester checks if the codeword reached maximum or minimum within the specified time period. Can't be too fast and can't be too slow.

7.4 DP Error Record

Field	Field	Description
next_sample	15…0	Error record is output one cycle after error to provide the next codeword (as an additional analysis point)
curr_sample	31…16	Current sample where error was observed
prev_sample	47…32	Previous code word sample.
average	63…48	Median point of codeword range. Calculated by tester
max_pt	79…64	Maximum point of codeword range. Calculated by tester
min_pt	95…80	Minimum point of codeword range. Calculated by tester
difference	111…96	Equation (1) calculation
avg_max_error	113…112	Unused
min_avg_error	115…114	Unused
avg_min_error	117…116	Unused
max_avg_error	119…118	Unused
diff_error	120	Indicates that sample difference is the error
out_timeout	121	Unused
max_timeout	122	Indicates that sample never reached maximum value
min_timeout	123	Indicates that sample never reached minimum value
avg_timeout	124	Indicates that sample never reached average value
out_max_error	125	Indicates that sample is larger than maximum bound

out_min_error	126	Indicates that sample is less than minimum bound
Debug	127	Dump or print
nx_error_count	143…128	Running count of the number of errors observed during testing.
out_flag	144	Unused
max_flag	145	Unused
min_flag	146	Unused
avg_flag	147	Unused
avg_max_flag	148	Unused
min_avg_flag	149	Unused
avg_min_flag	150	Unused
max_avg_flag	151	Unused
Time Stamp	175…152	Cycle counter Time stamp. Must multiply by the DUT frequency to convert to time. Used to determine error burst sequences

7.4.1 DP SEU Cross Section Calculations

Calculating the SEU Cross Section for the LTC1864L chains is a simple process: Count the number of upsets and divide by the reported particle fluence. The LTC1864L reported cross sections in this study are per device. No differentiation of analog versus bit upsets are performed.

When there is a burst of data, the total fluence must be adjusted because upsets are not being captured during the inoperable burst period. Hence, the number of particles that the device experienced during said period is subtracted off of the total.

(4)

8. HEAVY ION TEST FACILITY AND TEST CONDITIONS

8.1 Facility and Ions

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility, 15 MeV/amu tune).
Flux: $1.0x10^4$ to $2.0x10^5$ particles/cm^2/s
Fluence: All tests were run to 1 x 10^7 p/cm^2 or until destructive or functional events occurred.

Table 6: LET Table

Ion	Energy (MEV/Nucleon)	LET (MeV*cm^2/mg) 0°	LET (MeV*cm^2/mg) 45 °
Ne	15	2.8	3.96
Ar	15	8.5	12.6
Cu	15	20.3	28.71

The LT1864L devices were irradiated with Neon, Argon, and Copper at normal incidence (0) and 45 degrees (yielding effective LETs values listed in Table 6: LET Table) at the Texas A&M University Cyclotron Single Event Effects Test Facility.

8.2 Device Settings

Test Conditions:

Test Temperature: Room Temperature

Power Supply Voltage: 3.3v I/O and 1.5V Core.

8.3 Tester Settings

Prior to irradiation, tester parameters must be determined. Such parameters are the user set conditions such as error windows or boundaries based on codeword values. As the user-set error bound increases, the sensitivity of the tester decreases. I.e. if the parameter is set to 43, then the tester will only be able to observe errors greater than 43. The voltage equivalent of the error bound indicates the sensitivity bound of the tester based on analog voltage input. I.e. fluctuations in voltage less than the specified voltage equivalent field in Table 7 will not be observed.

Table 7: User set Error bounds per test type with corresponding voltage equivalents

Test Type	Error Type	User Set Error Bound	Voltage Equivalent
SP 0V 0ms Sleep time	Errorbound (Equation 1)	5 thru 8 (device dependent)	76.3µV thru 122 µV
SP 0V 4ms Sleep time	Errorbound (Equation 1)	5 thru 8 (device dependent)	76.3µV thru 122 µV
SP 0V 40ms Sleep time	Errorbound (Equation 1)	5 thru 8 (device dependent)	76.3µV thru 122 µV
SP 2V 0ms Sleep time	Errorbound (Equation 1)	43	656 µV
SP 2V 4ms Sleep time	Errorbound (Equation 1)	43	656 µV
SP 2V 40ms Sleep time	Errorbound (Equation 1)	43	656 µV
DP 10MHz	Difference (Equation 3)	86	1.31mV

Because the SP 0V has the smallest user-set error bound, the test setup has the greatest sensitivity to upsets. The trade-off is that an analog input of 0V may not have the greatest susceptibility. Hence, a variety tests are required to analyze the LTC1864.

9. PRELIMINARY WSR HEAVY ION TEST RESULTS

9.1 Single Event Latchup (SEL)

The LT1864L devices were monitored for Single Event latchup under the above conditions listed in Table 6. Sharp rises in current during radiation testing signifies device Single Event Latchup (SEL).Each part was placed in the beam until a Single Event latch (SEL) event occurred or 10^7 ions/cm^2 – the beam fluence was then recorded. During our experiment, Single Event latchup events occurred, yielding a threshold SEL LET for latchup ≈ 3.9 MeV•cm^2/mg. No SEL was observed at 2.8 MeV•cm^2/mg.

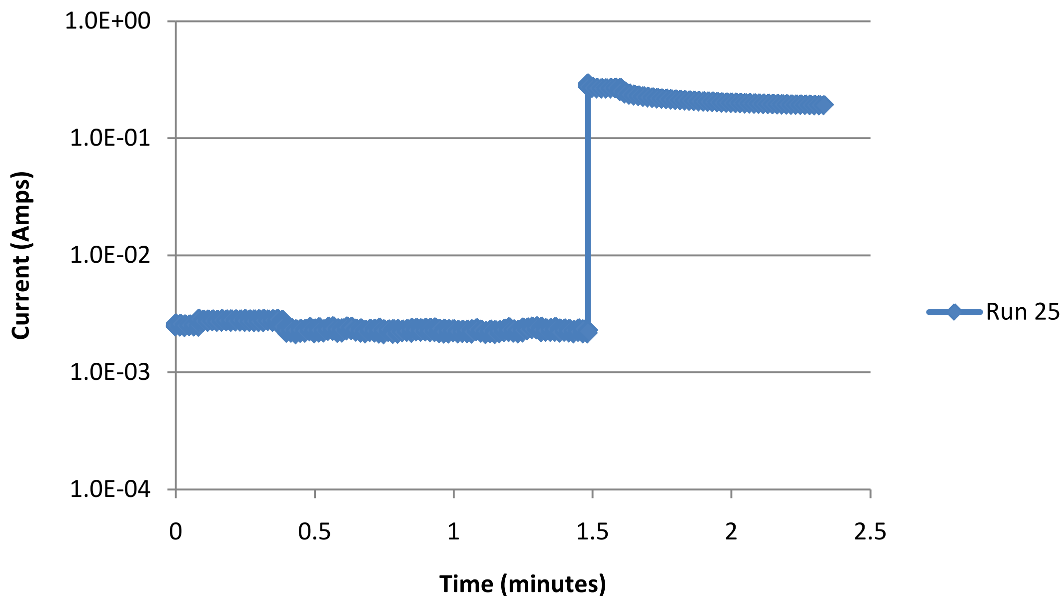

Figure 9: Single Event Latchup at LET=3.96MeV*cm^2/mg. Static analog input = 0V. SEL current increase is approximately 100x.

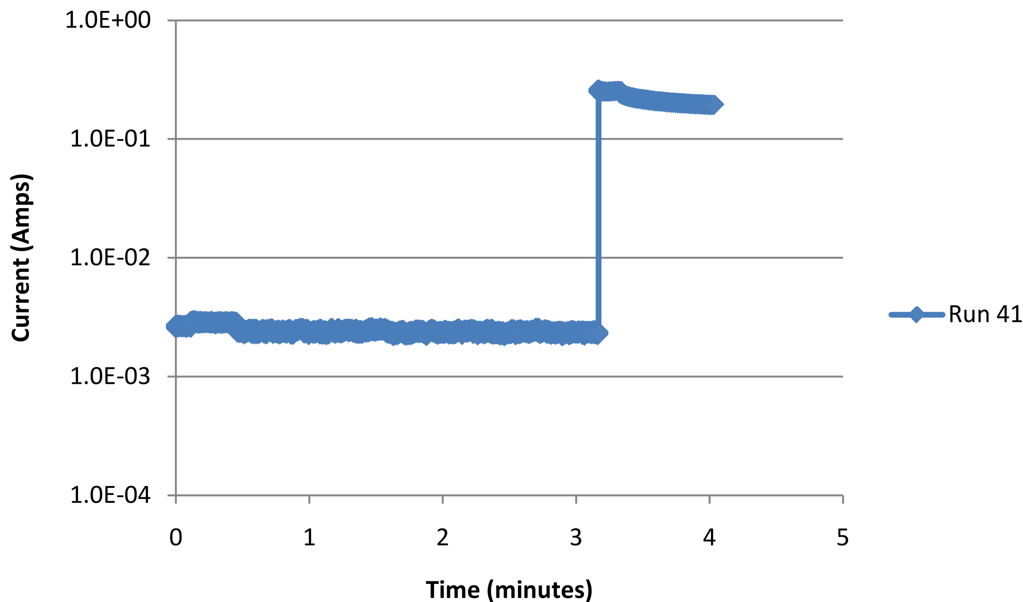

Figure 10: Single Event Latchup at LET=12.16MeV*cm^2/mg. Static analog input = 0V. SEL current increase is approximately 100x.

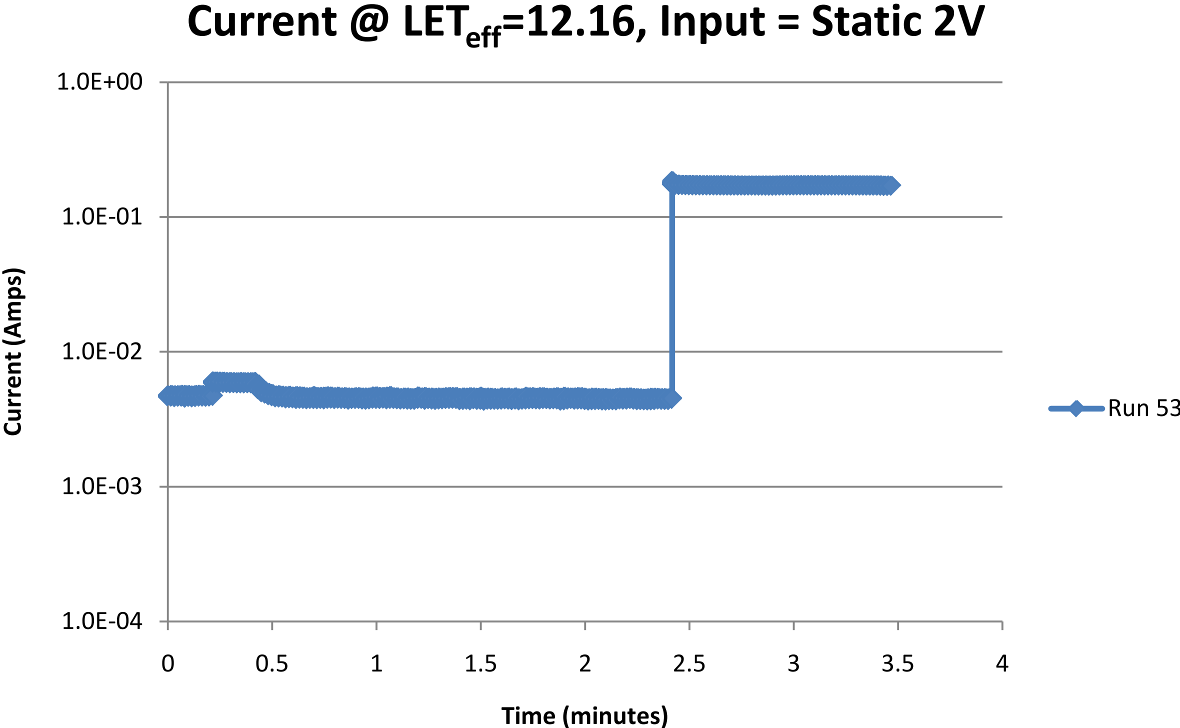

Figure 11: Event Latchup at LET=12.16MeV*cm^2/mg. Static analog input = 2V. SEL current increase is approximately 100x.

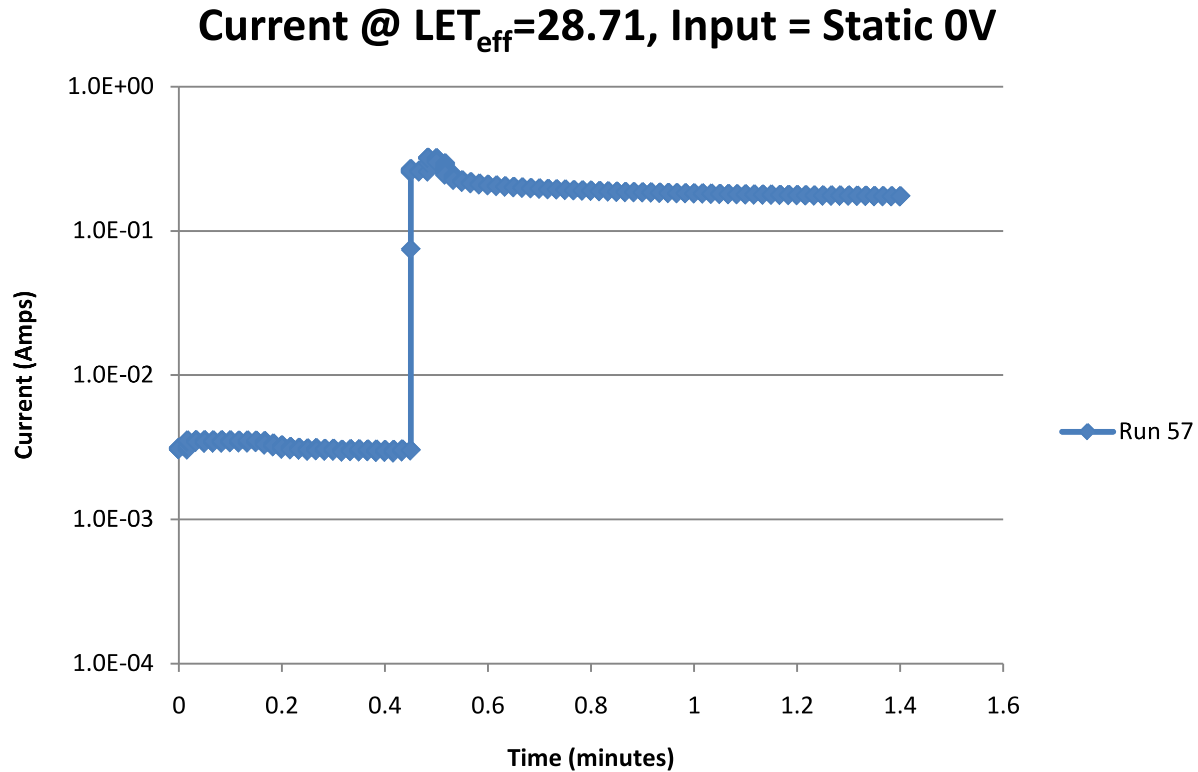

Figure 12: Event Latchup at LET=28.71MeV*cm^2/mg. Static analog input = 0V. SEL current increase is approximately 100x

9.2 Single Event Upsets (SEU)

As previously stated, user-set parameters were used within error determination for SEU calculations (see Equations 1-3 and Table 7). Because the test setup had the lowest amount of noise in the SP 0V analog setting, its error bound had the lowest value. In order to make comparisons between different test setups and test types that have different error bounds, the SEU results were run through filters. Filters are set such that only events with upsets greater than the filter value are reported. This provides a common reference point for test comparisons, however, errors are lost due to the inability to account for errors less than the specified filter. Filter values are listed in Table 8. An unfiltered SEU curve has upsets using the error bounds listed in Table 7.

Table 8: Filter Values and Analog Equivalents

Filter Value	Analog Equivalent
128	1.95mV
256	4mV
512	8mV

It is shown in Figure 13 that the bulk of errors are found in the unfiltered test set. Hence most of the upsets are smaller than 128 (or 1.95mV)

9.2.1 SP SEU Results

The following figures illustrate SP tests LET versus SEU cross sections (cm^2/device). Because upsets can occur in analog circuitry and digital and differentiation is complex in a random type test such as heavy ions, the SEUs reported are per device.

Figure 13 demonstrates SP with 0ms sleep time. There is a large number of upsets that fall under an error bound of 128. This suggests that a significant number of upsets occur in the analog circuitry.

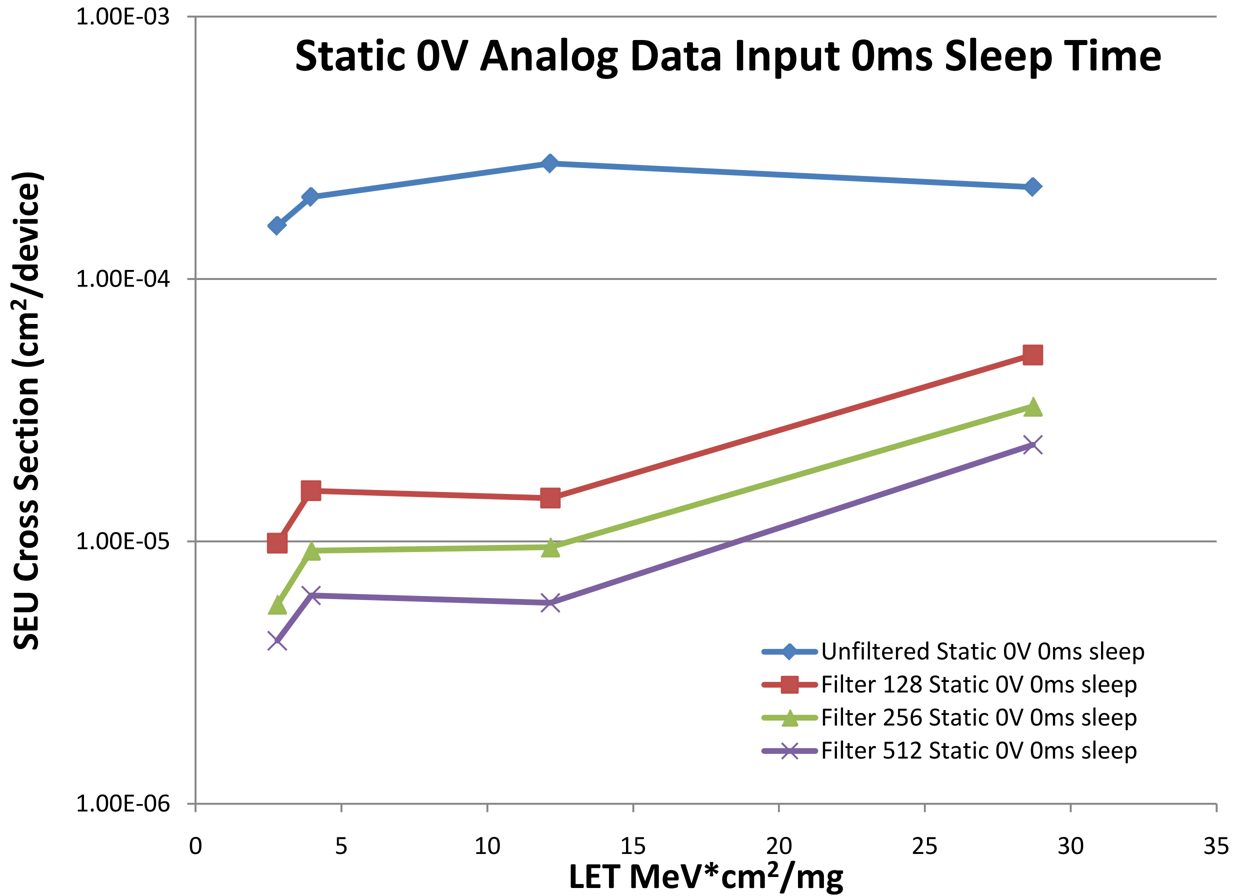

Figure 13: Static 0V Analog Data Input with 0ms Sleep Time. LET versus SEU Cross Section. Because of the small error bound, the unfiltered SEU curve is significantly higher than the filtered curves.

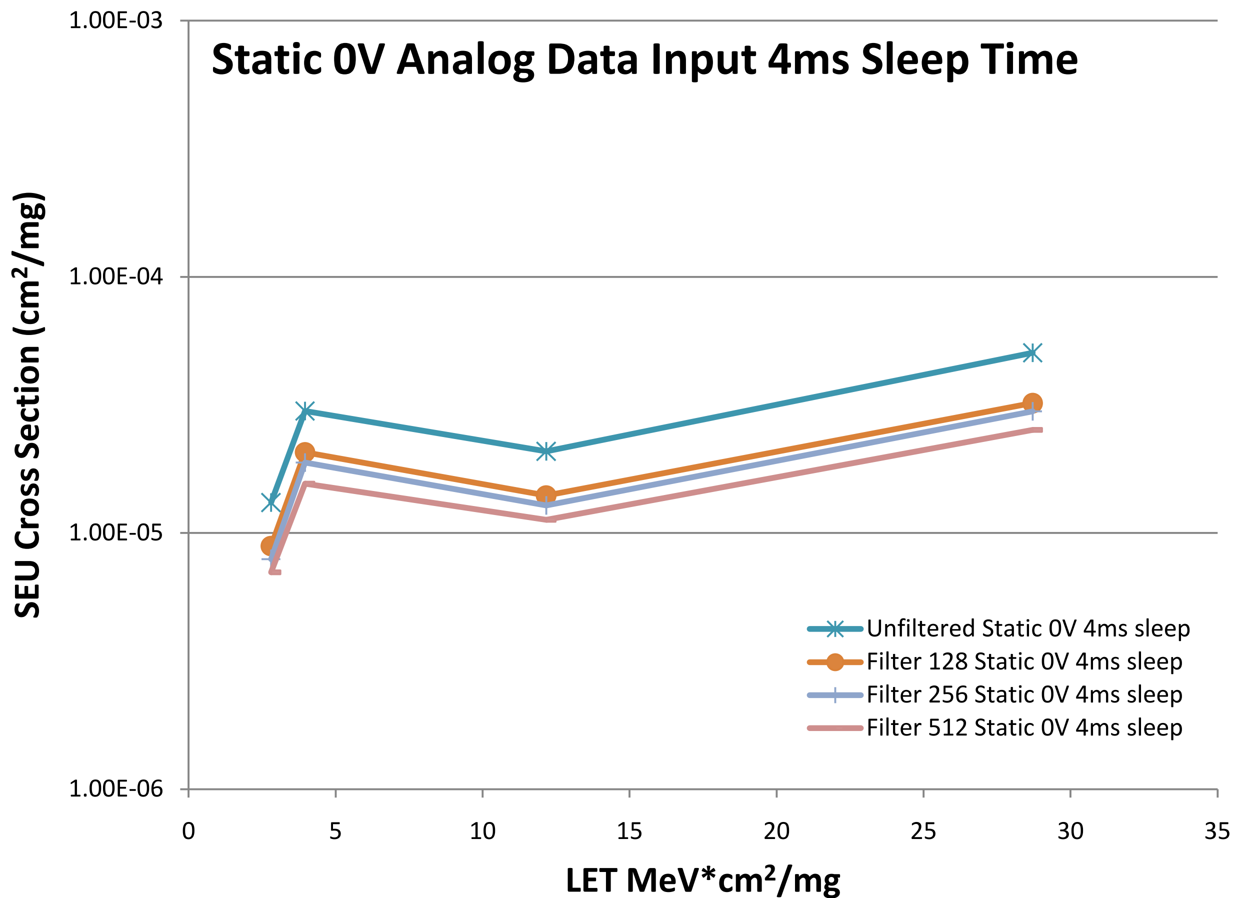

Figure 14: Static 0V Analog Data Input with 4ms Sleep Time. LET versus SEU Cross Section. Because there is not a significant difference between unfiltered and the other filters, upsets had relatively large values with 4ms. Upsets are assumed to be more digital than analog.

Figure 14 and Figure 15 demonstrate SP with 4ms sleep time. Because there is not a significant difference between unfiltered and the other filters, upsets had relatively large values with 4ms. More of the upsets are assumed to be digital than analog. The analog transients have time to dissipate during the 4ms sleep time.

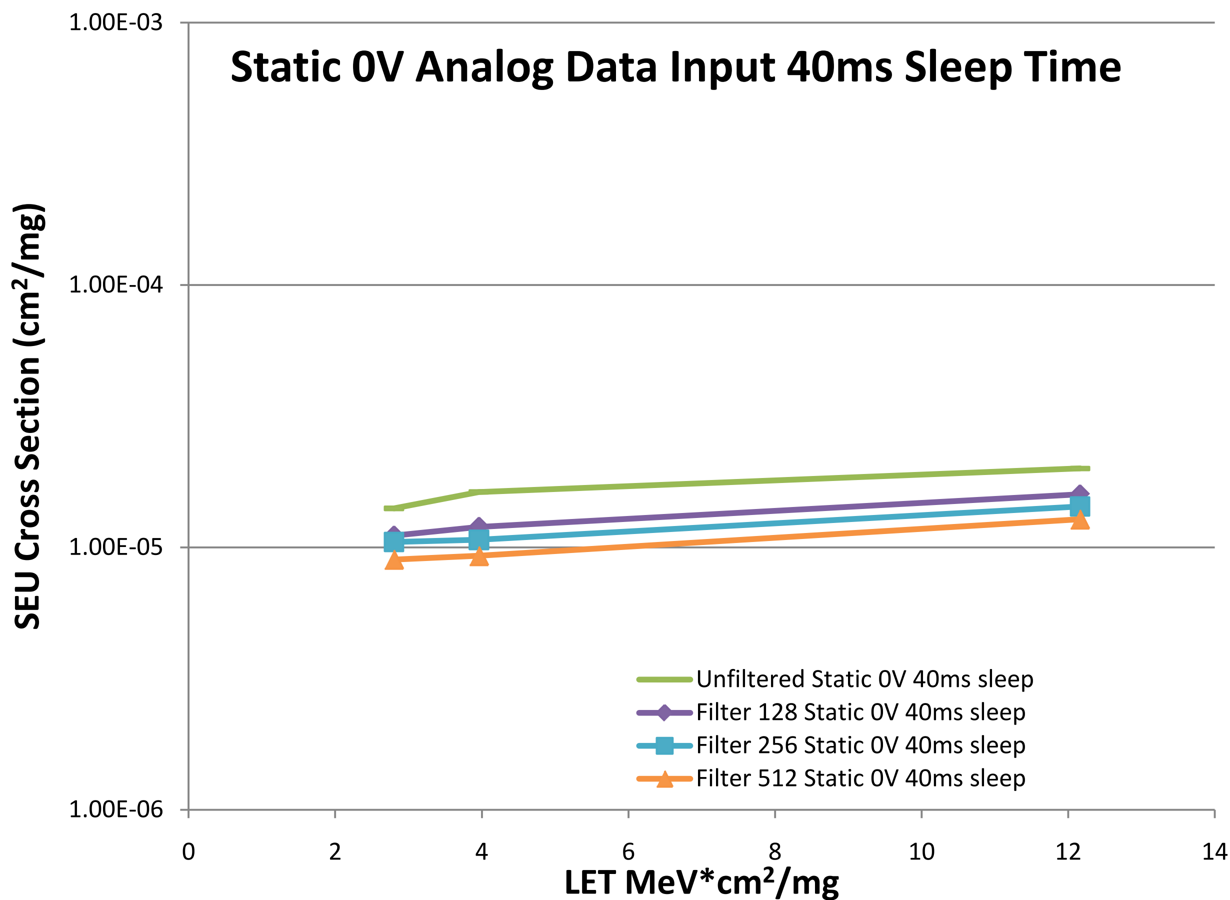

Figure 15: Static 0V Analog Data Input with 40ms Sleep Time. LET versus SEU Cross Section. Because there is not a significant difference between unfiltered and the other filters, upsets had relatively large values with 40ms. Upsets are assumed to be more digital than analog

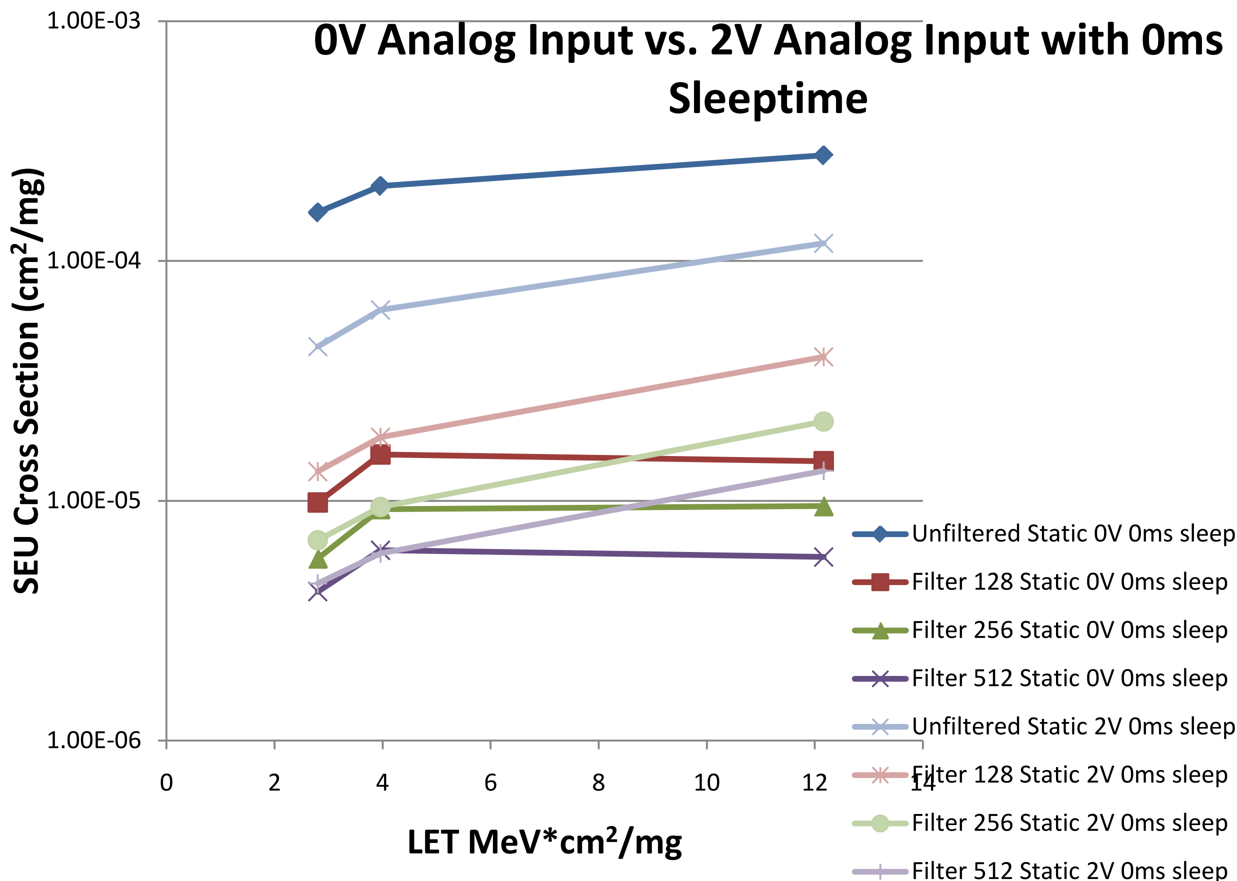

Figure 16: 0V versus 2V 0ms sleeptime.

Figure 16 and Figure 17 are a comparisons between 0V and 2V analog input. The 2V curves are lower than the 0V analog curves. This is because the 2V error bound is significantly larger than the 0V error bound. This suggests that the errorbound drives the difference in SEU cross sections and that if the test setup did not require a variation in error bounds, the SEU cross section for 0V would be similar to that of 2V. Hence, the analog input value does not have a significant effect on the SEU cross sections.

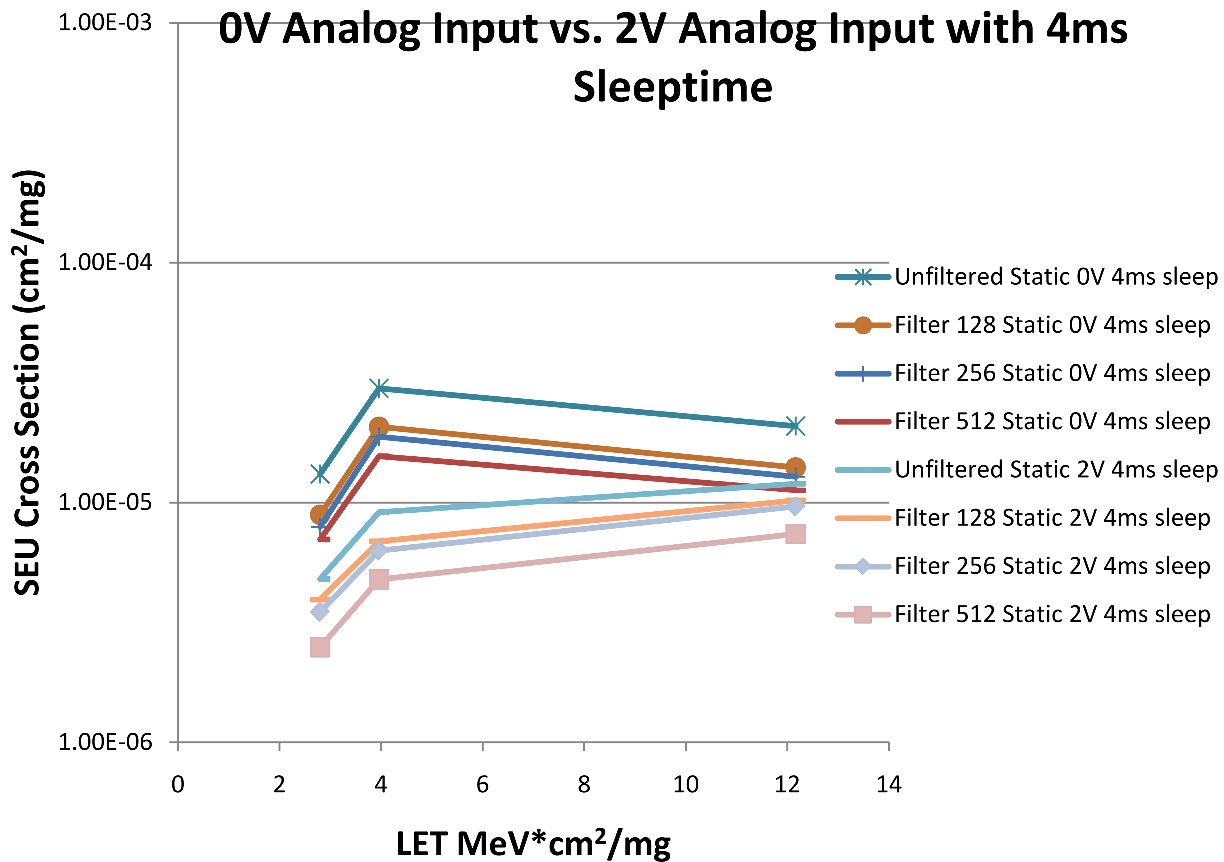

Figure 17: 0V versus 2V 4ms sleeptime

9.2.2 DP Heavy Ion Results

The DP method required the data input to slowly change over time. Although the data input voltage change was kept to a slow rate (10Hz cycle time), additional noise was injected into the test system. Consequently, the DP method required the largest error bound and hence had the least sensitivity to upsets.

Figure 18 shows the DP method SEU cross sections with filters for two LET values. As with the SP method, most of the upsets are under the 128 error bound value. Figure 19 compares the SP method to the DP method for 0ms sleep time.

The difference in tests is that the SP method requires a static input and a lower error bound. The DP method requires a slowly changing analog data input and a relatively high error bound. The SP method has the highest SEU cross sections because of its greater sensitivity to upsets. This implies that although the DP may seem more attractive of a test methodology because it traverses most input voltages and codewords, its decreased sensitivity to upsets makes it not as powerful as the SP test method.

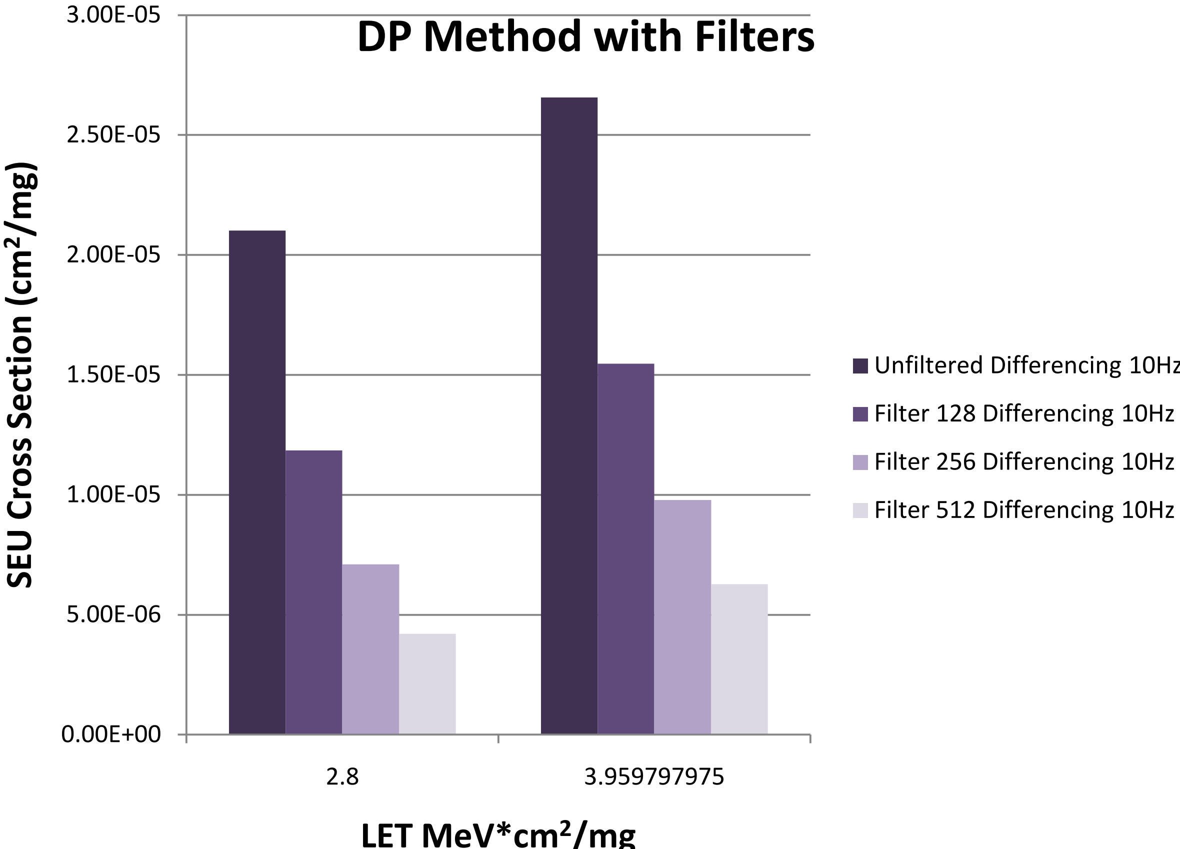

Figure 18: DP Method 0ms sleeptime with filtering.

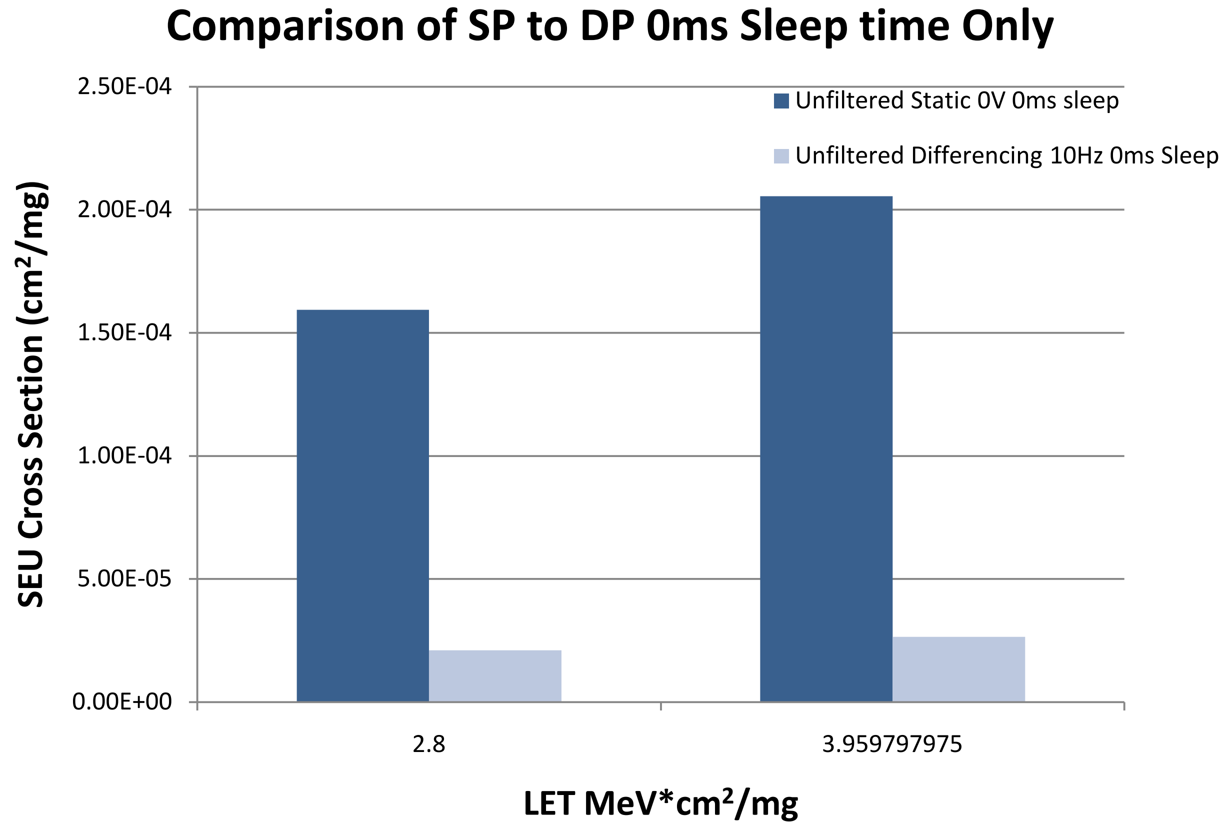

Figure 19: SP versus DP 0ms Sleep time SEU Cross Sections

10. CONCLUSIONS

The LTC1864 has a SEL $LET_{th} \approx 3.9$ MeV•cm^2/mg. SEUs were observed at all LET values, hence no SEUI LET_{th} can be assumed from this testing. A comparison between test methodologies suggests that the simplest test scheme (SP 0V data input) has the greatest sensitivity to upsets due to the low noise within its test setup. Based from this study, data input value did not seem to effect SEU cross sections. Hence, this serial ADC device is best tested using the SP 0V data input setup while varying sleep time.

11. APPENDIX 1:

[1] Actel Datasheet: "PROASIC/SL RadTolerant FPGAs" http://www.actel.com/documents/PROASIC_DS.pdf, V5.2, October 2007.