Synopsis V1.0
HI SEE Test Report for the Numonyx 4G NAND Flash Memory

Tim Oldham, Dell-Perot System Inc. /NASA-GSFC
Mark Friendlich, MEI Technology Inc./NASA-GSFC
Hak Kim, MEI Technology Inc./NASA-GSFC
Melanie Berg, MEI Technology Inc./NASA-GSFC
Kenneth A. LaBel, NASA-GSFC

Test Date: 5/22/2010 Report Date: 5/24/2010

I. Introduction

This study was undertaken to determine the susceptibility of the Numonyx NAND04GW3B2DN6 4 Gbit NAND Flash memory to destructive and nondestructive single-event effects (SEE). The device was monitored for SEUs and for destructive events induced by exposing it to a heavy ion beam at the Texas A&M University Cyclotron.

II. Devices Tested

We tested a total of 2 Numonyx NAND04GW3B2DN6 4G NAND devices marked with date code 831. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility.

The device technology is 73 nm minimum feature size CMOS NAND Flash memory. The chips came in a 48-pin TSOP package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface.

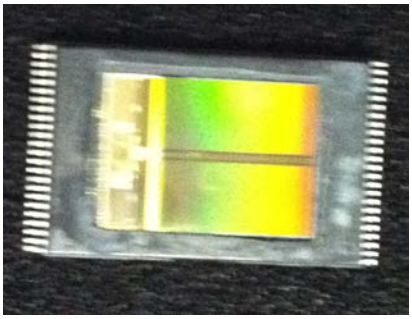


Fig. 1. Photo of die

III. Test Facilities

Facility: Texas A&M University Cyclotron
Flux: (3 x 10^3 to 1.0 x 10^5 particles/cm^2/s).
Fluence: All tests were run to 10^5 to 10^7 p/cm^2, or until destructive or functional events occurred.

Table I: Ions/Energies and LET for this test

Ion	Energy	Energy	Surface LET	Angle	Effective LET

	(MeV/amu)	(MeV)	(MeV/mg/cm^2)	(degrees)	(MeV/mg/cm^2)
Ne	15	300	2.8	0	2.8
Kr	15	1260	31	0, 45	31, 43.4
Xe	15	1935	56	0, 45	56, 78.4

IV. Test Conditions

Test Temperature: Room Temperature
Operating Frequency: (0-40 MHz).
Power Supply Voltage: 3.3V.

V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Available test patterns included all 0's, all 1's, checkerboard and inverse checkerboard, which were used to verify that the parts were fully functional before the test. Testing was done with the checkerboard pattern (AA) loaded. The effect of an ion hitting a cell is usually to cause zero-to-one errors—loss of electrons off the floating gate. But control logic errors can cause errors of either polarity, and the AA pattern allows us to detect these errors. The maximum clock frequency for these devices was 40 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern (AA) was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

3) Dynamic Read, in which a pattern (AA) was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read. In this test, we skipped this test mode most of the time, because of limited beam time, and because the results have sometimes been difficult to interpret in other tests.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.

6) In general, it was also intended to conduct latchup testing at 70° C, and 3.6 V, but such testing is time consuming, in that it takes time for the samples to come to equilibrium at the high temperature. Because of limited beam time, we did not attempt high temperature testing, in this case. The DUTs were monitored for latchup in the tests actually conducted, at room temperature, and no SEL was observed, but this is not a realistic worst-case test condition.

The Block diagram for control of the DUT is shown in Figure 2. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the flash is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for over-current conditions and shuts down power to the DUT if such conditions are detected.

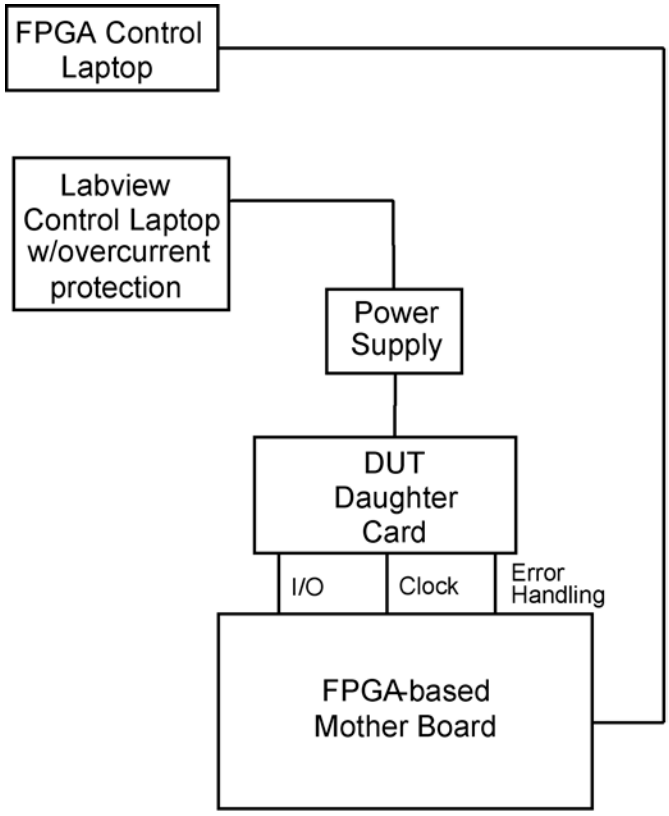
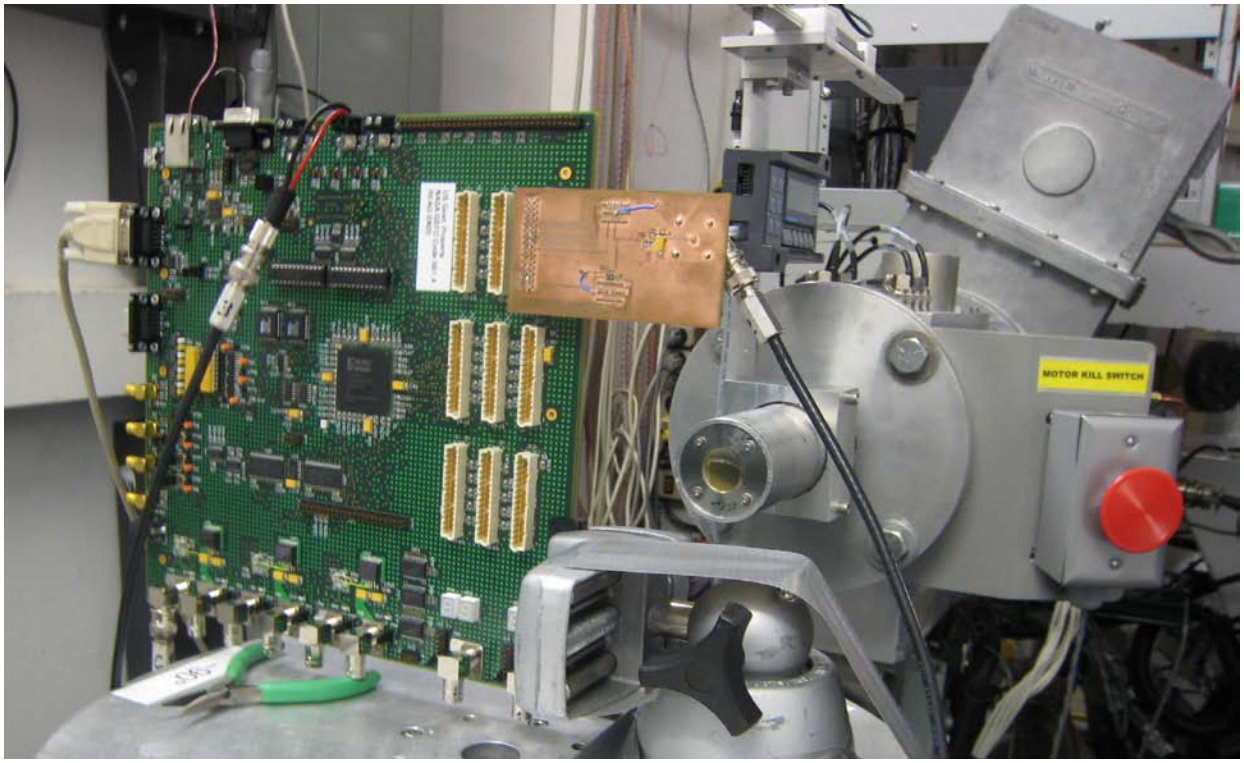
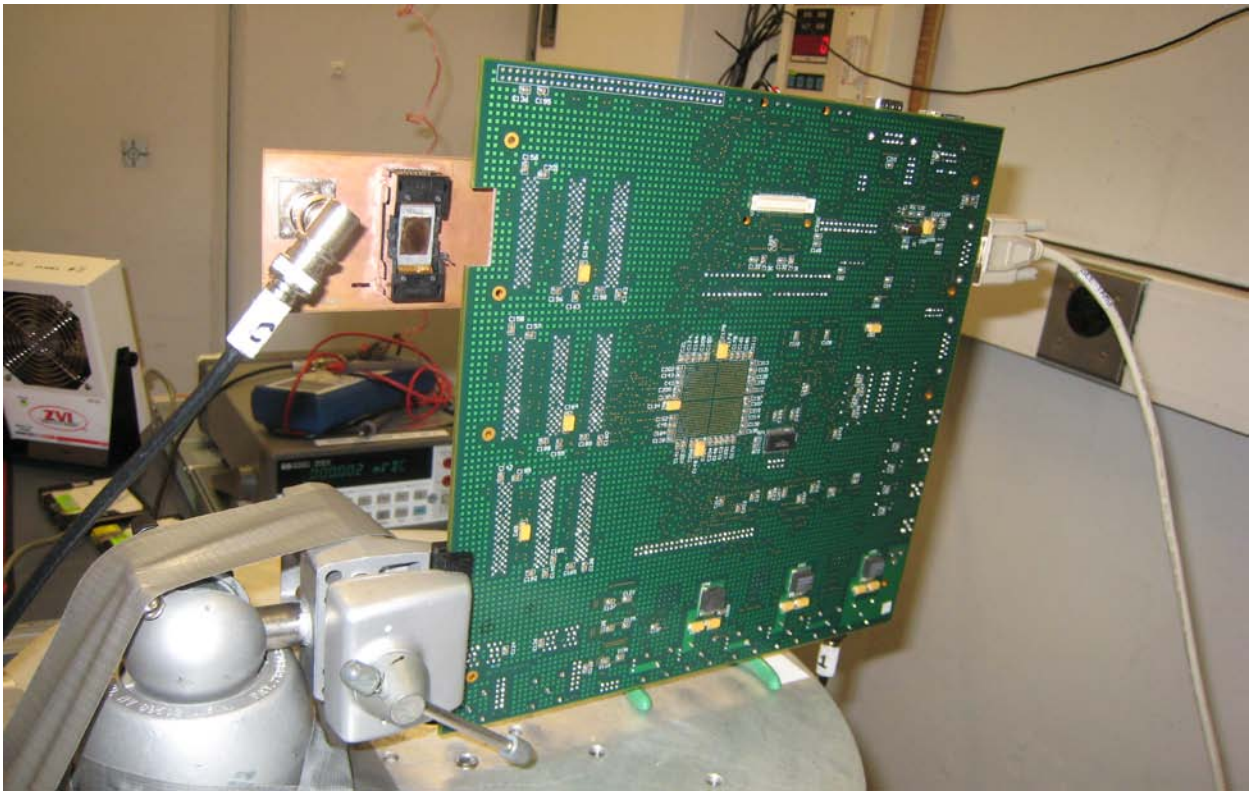


Figure 2. Overall Block Diagram for the testing of the Numonyx NAND Flash.



(a)



(b)

Fig. 3. (a) Front and (b) back views of motherboard and daughterboard, with DUT.

VI. Results

During testing, the NAND04GW3B2DN6 was irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam, except as noted. The errors observed in static testing, without bias, are shown in Fig. 4. In Fig. 4 and other Figures, we plot results obtained at angles other than normal incidence using the "effective" LET, in order to separate the normal incidence shots from those at other angles. We recognize there are sometimes pitfalls associated with the use of effective LET for other purposes. There were no SEFIs on any zero bias shot, and the results in Fig. 4 are just single bit errors.

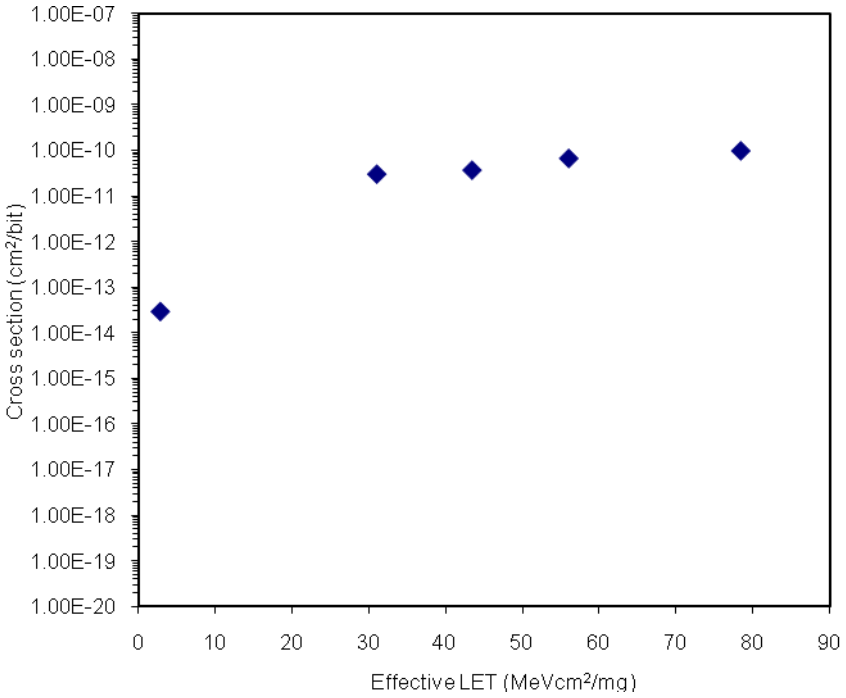


Fig. 4. Measured error cross sections in static unbiased mode.

Results for static mode, with bias, are shown in Fig. 5. Here and in the following discussion, bit errors are taken to be single bits, which are flipped, as a result of the interaction with incident ions, normally from zero to one. We do not have the physical to logical address mapping, which would allow us to look for multiple bit errors (error clusters) for these parts. However, in the overwhelming majority of cases, there is only one error in a page, or one error in an entire block, which makes it extremely unlikely that there will be multiple errors from a single ion. This result is consistent with previously published results on the upset mechanism in flash memory—an ion passing through a floating gate creates a dense charge column, which creates a conducting path between the gate and substrate, which allows charge to leak off the floating gate. Since the ion only hits one gate, only one bit is affected. This situation is far different from that in volatile memories, where charge generated in the Si substrate can be shared across multiple nodes.

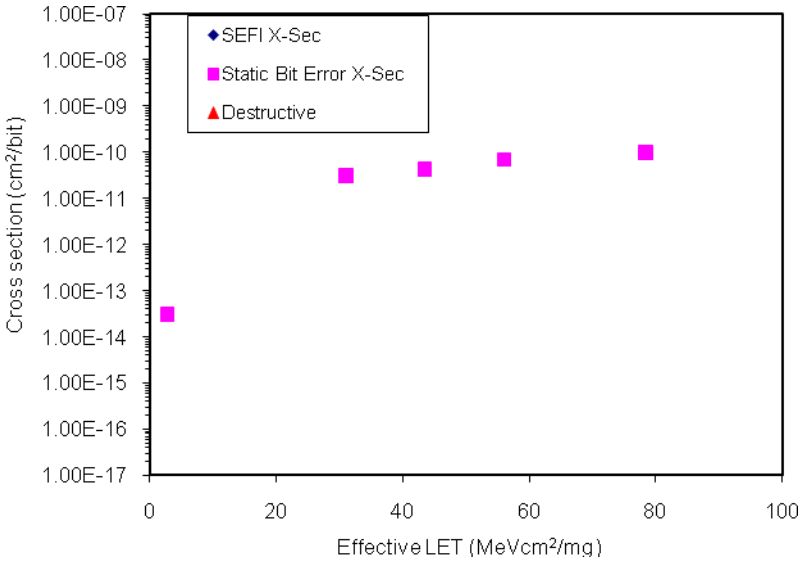


Fig. 5. Error cross-sections observed in static mode, with bias.

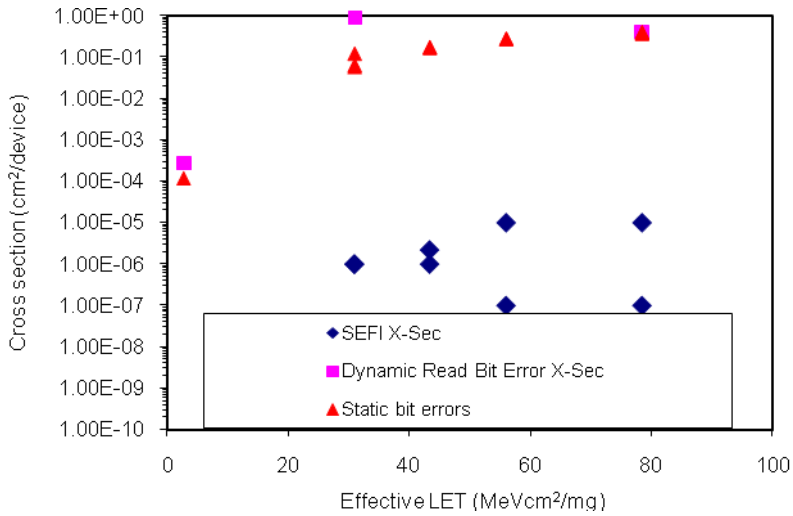


Fig. 6. Dynamic read error cross sections.

For the Dynamic Read condition, the parts showed exhibited transient read errors in addition to the bit and Page/Block errors, and other SEFIs, which are plotted in Fig. 6. Generally, in this mode, there are static errors, which are determined here by reading after the beam has been turned off, and the power cycled. Transient errors includes errors resulting from transient noise in the read circuit, but since the part reads continuously, multiple reads of static errors may also be included as transient errors. On all but three shots in this mode there was a SEFI, which made it impossible to determine the transient errors, in any case.

We took only one shot in the dynamic R/W mode, because the results have often been difficult to interpret in the past. In this case, there was a major SEFI on that shot, so it was impossible to tell how many real errors there were, except for static errors after a power cycle. The static error rate was consistent with the static mode shots.

Results for the dynamic R/E/W tests are shown in Fig. 7. In this mode, the part reads continuously, except that when errors are detected, they are erased and rewritten. The bit errors are counted as they occur, but they are reset, so there are no static errors left after the beam is turned off. The error count here is similar to the static error count in other test modes. There was a SEFI on all shots but one in this test mode, but the SEFI modes have not yet been analyzed in detail. There was one functional failure in this mode, which was due to the loss of the erase function. The failure occurred on the twelfth shot with Xe ions (LET approximately 56), when the total fluence was more than 2.2×10^7 particles/cm^2. We note that the flux at this LET for the Adams Worst Case Environment is less than 1 particle/cm^2 per hundred years, so this fluence is equivalent to more than two billion years in geosynchronous orbit. We do not claim great statistical significance for this result, because it was obtained on a single sample. But it took the entire beam run to get a single failure, so the reliability of these parts appears to be promising for space applications.

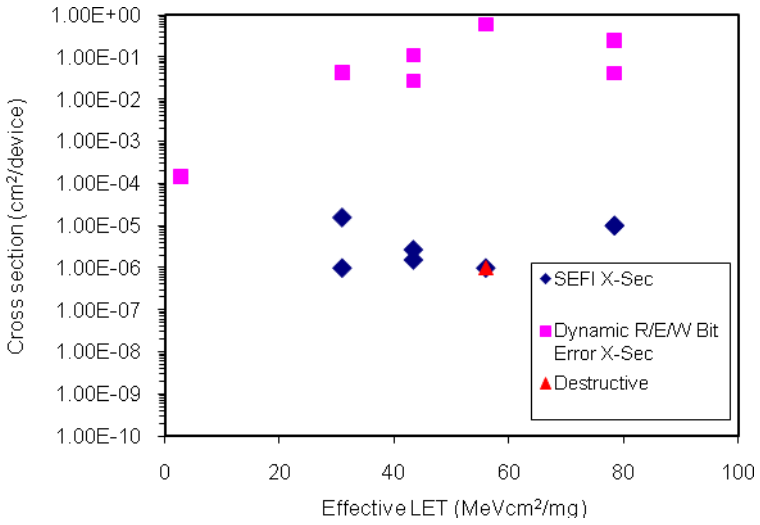


Fig. 7. Error cross sections for dynamic R/E/W test mode.

All the testing was done at room temperature, which is not a worst-case condition for SEL (single event latchup). However, we did monitor the DUTs for SEL, and no SEL was observed.

VII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the Numonyx NAND04GW3B2DN6 4-Gbit NAND. Although the static bit error rate is projected to be very good in space, additional testing is required before these devices can be considered for space applications. In particular, SEFIs will need to be better understood, and mitigation strategies identified.