Achronix SPD60 Heavy Ion Single Event Effects Test Report

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1. INTRODUCTION

This study was undertaken to determine the single event destructive and transient susceptibility of the Achronix SPD60 Field Programmable Gate Array (FPGA). The SPD60 has a SRAM based configuration and is an asynchronous (hand shaking) FPGA. The devices were monitored for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing them to a heavy ion beam at the Texas A&M University Cyclotron Single Event Effects Test Facility.

2. DEVICES TESTED

The Speedster (SPD60) devices were manufactured on a proven TSMC 65 nm CMOS process. The manufacturer is Achronix. Due to noise issues, only one device was placed within the heavy ion beam for testing.

Lot and date code: 0921

Serial Number: 17

The following are some of the SPD60 Features.

- Very fast FPGA
  - 1.5 GHz system performance
  - SRAM-based FPGAs
  - Field reprogrammable
- Up to 1.5 Million ASIC gates
- 1.5 GHz 18Kb RAM blocks
- Up to 40 lanes of embedded 10.3 Gbps SerDes
- 10.3 Gbps SerDes, supporting:
  - Gigabit Ethernet
  - PCI-Express Gen1 & Gen2
  - CEI-6G
  - 10 Gbps Backplane
  - Infiniband
  - XAUI
  - XFI
- Industry standard Memory interfaces supported:
  - DDR1 SDRAM (400 Mbps)

  - DDR2 SDRAM (800 Mbps)
  - DDR3 SDRAM (1066 Mbps)
  - SDR SDRAM (200 Mbps)
  - QDR SRAM (400 Mbps)
  - QDRII SRAM (800 Mbps)
  - RLDRAM II (1066 Mbps)
- Industry standard datapath interfaces supported:
  - PCI/PCI-X (33-133 Mbps)
  - SPI-4.2 (Up to 1000 Mbps)
  - SFI-4.1 (622 Mbps)
  - XSBI (644 Mbps)
  - Hypertransport 1.0 (800 Mbps)

3. TEST PROCEDURES

All Heavy Ion radiation tests were preformed at the Texas A&M Cyclotron Facility. The following sections describe various types of tests and how they were performed by the user.

3.1 Configuring the DUT via the Tester

Because the Achronix SPD60 has SRAM based configuration, the user must write the configuration memory prior to every radiation test. The DUT had a direct connection to the host PC and was configured via JTAG. The Test Setup is depicted in Figure 1.

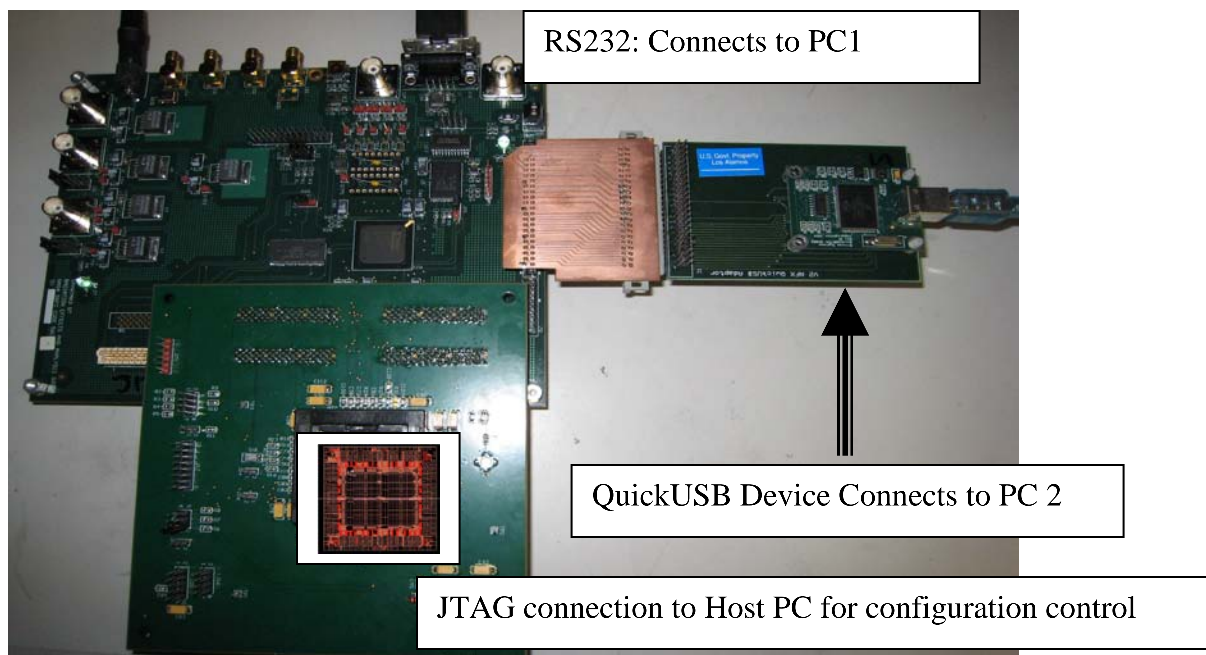

Figure 1: Tester and SPD60 DUT Board (must be updated for current board)

3.2 After Configuration: Running a test

After sending the test parameters and successfully configuring the DUT, the start test command was sent. The beam was turned on after the start test command. Tests were run until a fluence of $1e^4$particles/cm^2 to $1e^6$particles/cm^2 was reached, or a significant number of upsets were captured, or unrecoverable error is detected. The LabView user interface guided test time. Particular attention was paid to DUT current monitoring. A rise in current that could compromise board components dictated when tests were halted. The following describe the types of tests that were performed: Static and dynamic.

3.2.1 Static Testing – Configuration Evaluation

Static tests were performed to evaluation the integrity of the configuration memory of the DUT . Errors were determined by reading back the configuration memory after irradiation and comparing each bit to the expected bit stream. The procedure was as follows:

- Power down/reset Tester and DUT
- Configure DUT via JTAG
- Verify configuration is successful via Host PC
- Store verify readback file corresponding to test number
- irradiate DUT and monitor current during radiation.
- stop beam and readback configuration of DUT via Host PC
- store readback file and note number of bit errors
- The static bit error cross section was calculated as:

$$\sigma_{error} = \frac{\#errors}{ConfiguraitionSize * fluence}$$

Achronix SPD60 *ConfigurationSize* `= 67,108,804 (65536 x 32 x 32).`

3.2.2 Dynamic Tests

3.2.2.1 General Description

Dynamic Tests were performed to specifically evaluate the DUT fabric switching components (both asynchronous and synchronous). Inputs are controlled by the LCDT and DUT outputs are monitored by the LCDT for potential error. An error is logged if the DUT output does not match the expected value.

Input Sequence	Expected Output
Checker Board	Tester will synchronize to the checker board ordering at test commencement and upon error
All 0	Output will always be 0 – no synchronization is required to output values
All 1	Output will always be 1 – no synchronization is required to output values

3.2.2.2 Architectures

The following are the windowed shift register variations that were tested:

1. Windowed Shift Register with 0 Combinatorial blocks between Sequential Stages
2. Windowed Shift Register with 8 Combinatorial blocks between Sequential Stages
3. Windowed Shift Registers with 16 Combinatorial blocks between Sequential Stages

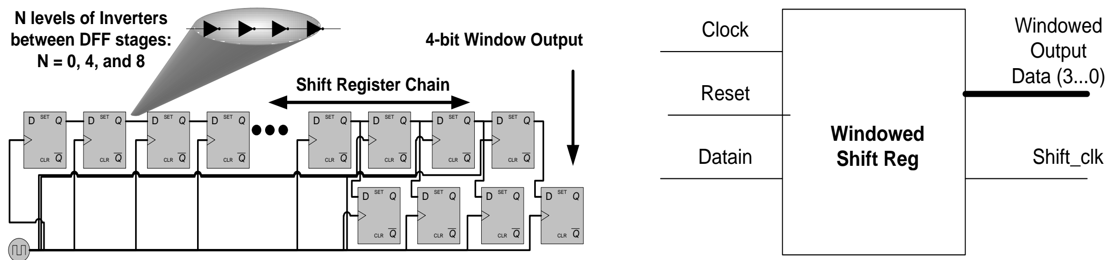

Figure 2: Windowed Shift Register

3.2.2.3 Procedure

The procedure is as follows:

- Reset Tester and DUT
- Configure DUT via JTAG
- Verify configuration is successful via Host PC
- Store verify readback file corresponding to test number
- Start operation (clocks and data toggle) and start monitoring (validate operation prior to irradiation)
    - Monitor the shift_clk and
    - Monitor data outputs of the windowed shift register
    - Monitor system current.
- irradiate DUT and monitor outputs
- stop beam and stop test

#DFFBits refers to the analogous SEQ circuitry (expected number of flip flops) in the SPD60 asynchronous fabric in the following equation.

$$\sigma_{error} = \frac{\#errors}{\#DFFBits * fluence}$$

4. HEAVY ION RADIATION TESTS AND RESULTS

Heavy Ion radiation tests were performed at the Texas A&M Cyclotron Facility. The following are the effective LETs during irradiation: 0.94, 1.3, 1.9, 2.0, 3.0, 6.4, 9.6,15, 24.6, and 49.3. The DUT was positioned at normal incidence and at 45 degrees.

See attached excel sheet for details of each test.

4.1 Radiation Data Integrity

During debug, it was discovered that the SPD60 core Voltage was not connected to its supply. A quick fix was implemented using a wire to connect. After the new wiring, the device I/O were very noisy. This could have been a repercussion of the core voltage wire or faulty socketing connects. The cause is still not determined. In order to obtain a working environment, the number of I/O were reduced. This actually increased the signal integrity such that some of the tests could be run. More specifically, the static configuration tests were reliable (no noise was observed on the I/O pertaining to the configuration interface).

Regarding the dynamic shift register tests, there was still too much noise at the time of testing on the pins that connected to the shift register strings. Further debug after testing helped to find a reliable I/O list. Because of this, dynamic shift register tests (although performed) are deemed unreliable.

As a summary, dynamic shift register tests are considered unreliable data while configuration readback tests all prove to be reliable information. This does not compromise device characterization because the large number of configuration upsets and the inability to scrub the configuration memory also impaired dynamic operation during irradiation.

4.2 Configuration Readback Bit Upsets

The attached excel sheet contains the number of configuration bit upsets per test. Further analysis suggests a significant number of bit upsets are MBUs at higher LETs. This could be potential control logic Single Event Transients (SETs). Some tests at high LETs contain more bit upsets than particle fluence.

The analysis of configuration upsets included identifying single bit upsets and upsets due to control line transients. See Figure 3.

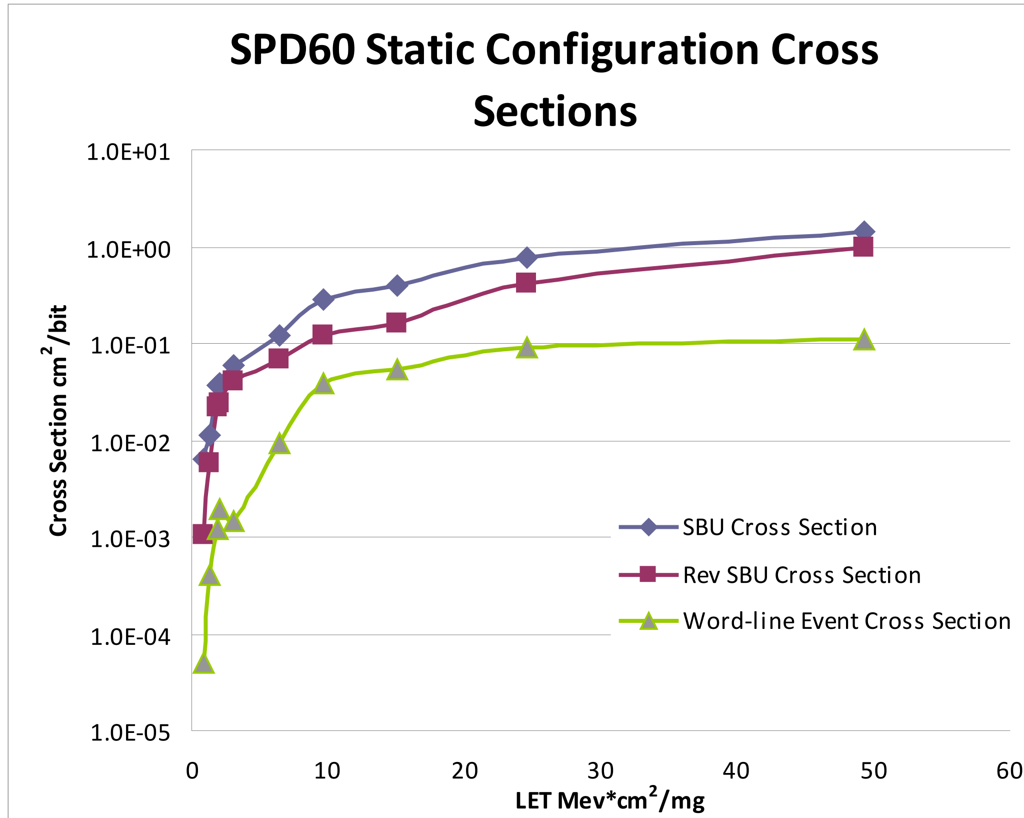

Figure 3: Configuration Memory SEU Cross Section. SBU – Single Bit Upsets; REV SBU – distinct upsets (Potential MBUs are combined into one upset); Word-line – potential control logic SEUs that affected many bits.

4.3 Single Event Latch-up

Tests that contained a large amount of bit upsets also experienced sharp current jumps. This is more than likely not SEL but many configuration bits in the wrong state causing contention within the fabric. This same phenomenon has been witnessed with configuration-bit fault injection in other SRAM Based FPGA devices. Discussions with the manufacturer also support the contention theory. However, it should be noted that SEL is a possibility. It is difficult to prove from the completed testing because prior to DUT re-configuraiton, a powerdown was performed. Differentiating if a power cycle was required to lower the current or if a re-configuration would have solved the problem is not possible at this time. If all is required is a reconfiguration, then SEL would not be the cause of the current jumps – it would be contention due to bit upsets. Subsequently, future testing must include a reconfiguration prior to power cycling in order to come to a conclusion on SEL versus contention.

5. SUMMARY OF TESTING

Board debug time was limited prior to testing. Consequently, the integrity of the radiation data obtained during the TAMU test trip can only be guaranteed for configuration bit upset evaluation.

Configuration MBUs (or configuration control line upsets) and large current jumps were witnessed during testing. Further testing is required to further investigate the cause of the upsets. Additional analysis will also require the assistance of Achronix to interpret the source of MBUs.