Test Report V2
Single Event Effects (SEE) Testing of the 7872ARPFS
14-bit Analog to Digital Converter

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## I. Introduction

The 7872ARPFS is a 14-bit analog to digital converter (ADC). This part is designed in the advanced LC$^2$MOS process. This process gives an increased signal capability of $V_{SS}$ to $V_{DD}$ and enables operation over a wide range of supply voltages. The ADC has been tested at Texas A&M University Cyclotron Single Event Effects Test Facility. Three devices were tested for SEE.

## II. Devices to Be Tested

The 7872ARPFS devices were designed and fabricated by Analog Devices, Inc. They are fabricated in the advanced LC$^2$MOS process, and are intended to be packaged by MSKennedy. All devices were characterized prior to exposure. The three devices tested are from the 1008 Lot Date Code (LDC). Complete package markings for the devices are:

| |
|---|
| 68911 |
| 7872ARPFS |
| RAD.PAK® |
| 1008 USA Δ |

Table 1: Packaging information

These are all 16 pin devices in a CerDIP package. The actual devices are shown in the Figure 1.

**Product Datasheet:** 7872ARPFS.pdf

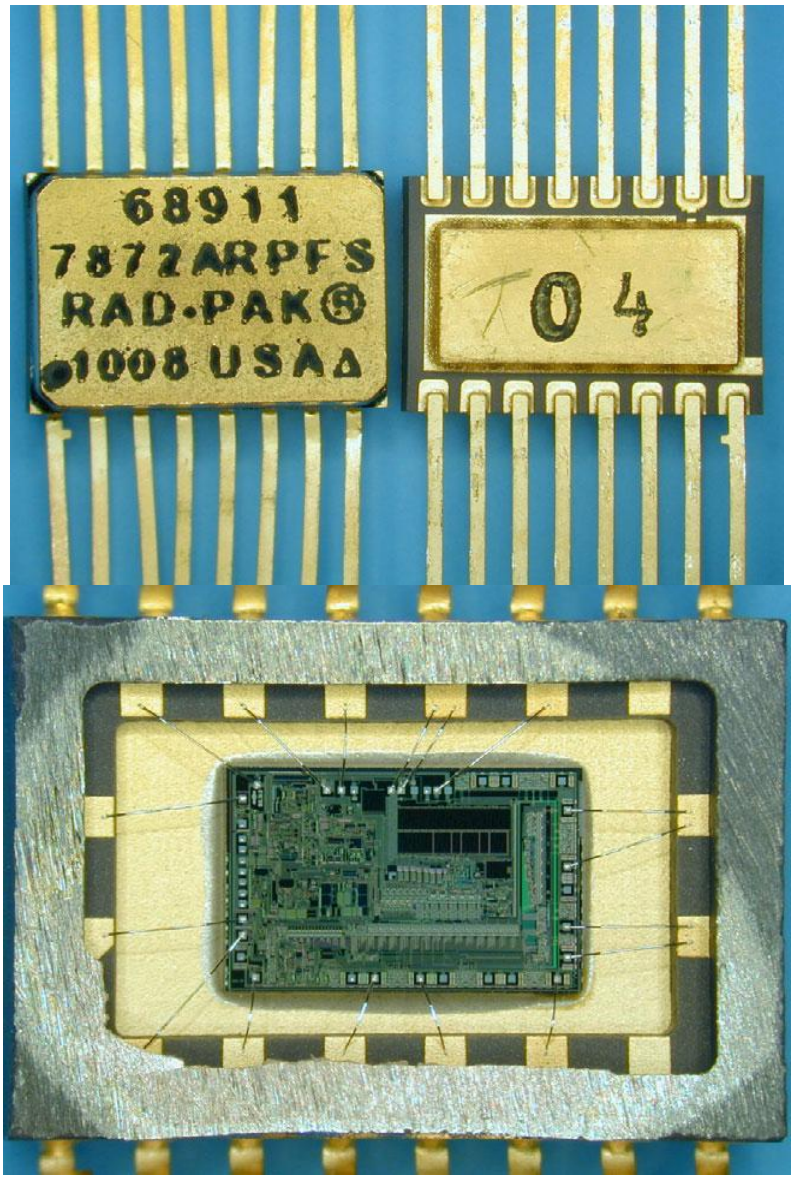

Figure 1: Picture of the 7872ARPFS before (top) and after (bottom) being de-lidded.

## III. Test Facility

**Facility:**
TAMU Cyclotron Single Event Effects Test Facility, using the 15 MeV/amu tune

**Total Beam Time:**
8 hours

**Flux:**
5 x $10^2$ up to 8 x $10^4$ p/cm$^2$/s

**Minimum Fluence Achieved Per Part:**
1 x $10^7$ p/cm$^2$

| Ions used (angle) | Air gap distance from rear foil (cm) | Effective LET ($MeVcm^2/mg$) |
|---|---|---|
| Ne (0) | 6.0 | 2.8 |
| Ne (30) | 6.0 | 3.23 |
| Ne (45) | 6.0 | 3.96 |
| Ne (60) | 6.0 | 5.6 |
| Ar (0) | 6.0 | 8.8 |
| Ar (45) | 6.0 | 12.45 |
| Ar (60) | 6.0 | 17.6 |
| Kr (0) | 6.0 | 29.6 |
| Kr (30) | 6.0 | 34.18 |
| Kr (45) | 6.0 | 41.86 |
| Xe (0) | 6.0 | 54 |
| Kr (60) | 6.0 | 59.2 |

Table 2: TAMU Ion information

## IV. Test Methods

**Temperature:**
Room temperature, >70C (Latch-up Test)

**Test Voltages:**
Nominal (5 Volts) supply, and -3V to +3V analog feed through.

**Operating Speed:**
40 kHz, 80 kHz

**Test Hardware:**

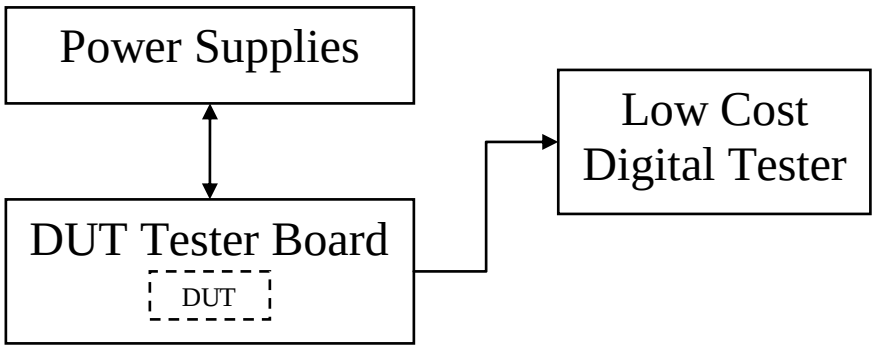


Figure 2: Block diagram of test setup where the dashed line represents the components exposed to the heavy-ion beam.

AD7872 Schematic Diagram

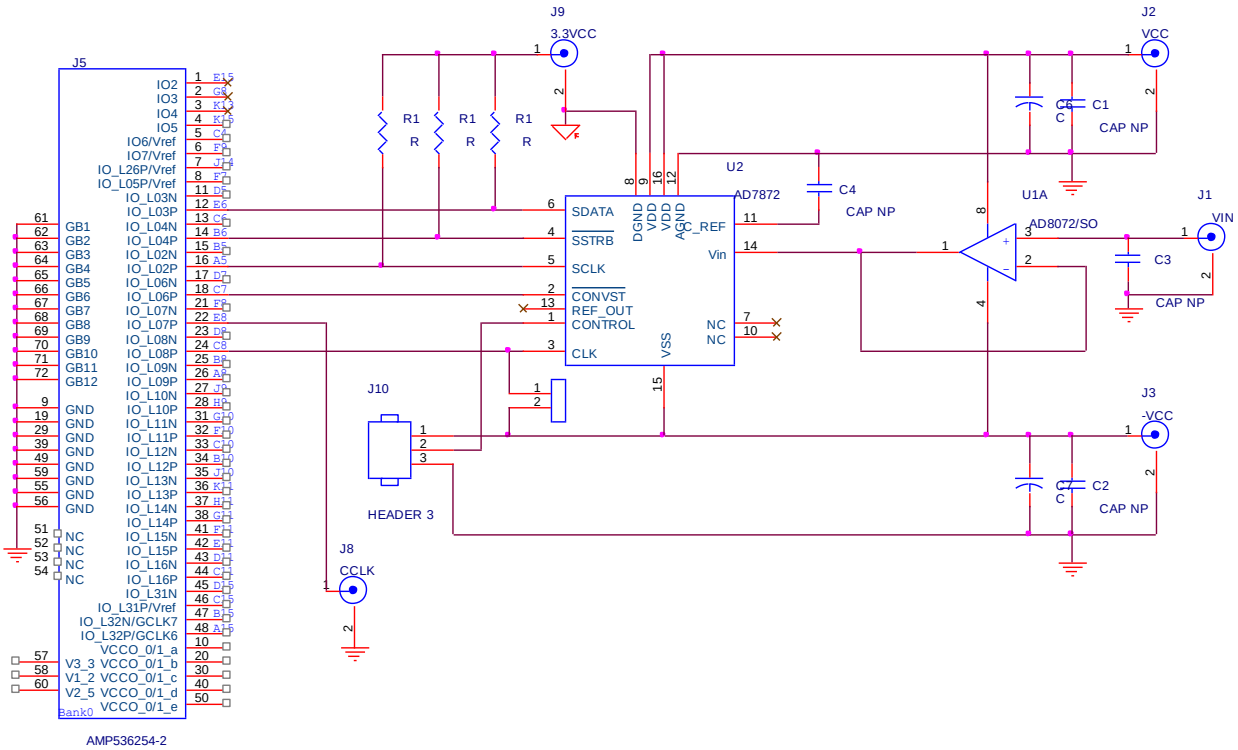


Figure 2: 7872ARPFS Daughter Card Schematic

## V. **Test Results**

SEU: A single event upset on the 7872ARPFS manifested itself in an unexpected discretization of the digital output from the device, i.e. the output was unexpected and did not return to an expected value. Events that resulted in the temporary loss of either the strobe line or the clock line, both responsible for framing and clocking in the 14 bits of the digital code, were also counted as SEUs. The effects of ion strikes to the digital output control circuitry for the output code largely resulted in SEUs.

SET: A single event transient on the device was characterized by the expected throughput being outside of the trigger window and returning back to an expected value. The SET was recorded and counted if the voltage level was outside of the expected window. For this test setup, transient deviations of +/- 14.6mV, or 40 LSBs, from the expected digital output were counted as SETs. The effects of ion strikes to the track and hold circuitry and to the analog comparator circuitry largely resulted in SETs.

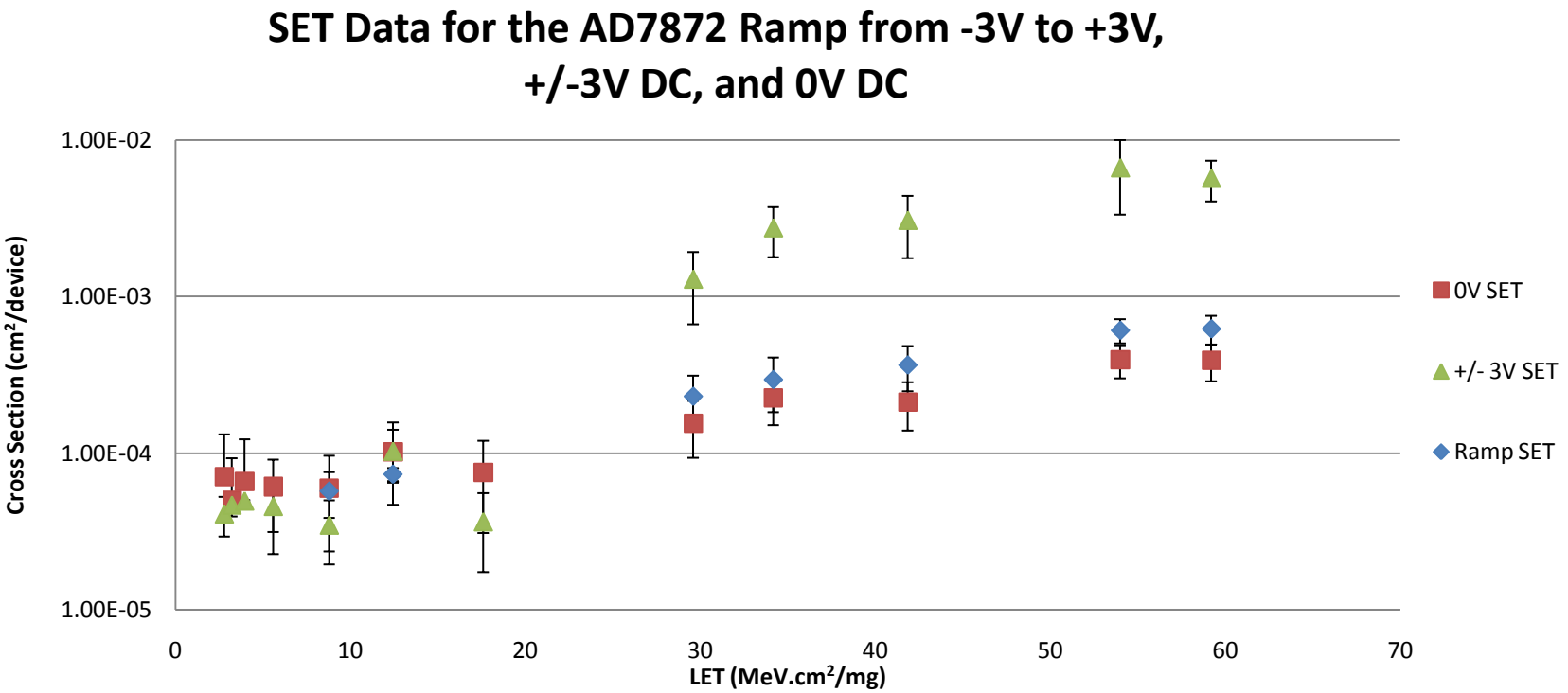


Figure 9: SET Cross section of the 7872ARPFS device shown with +/- one standard deviation bars at each LET

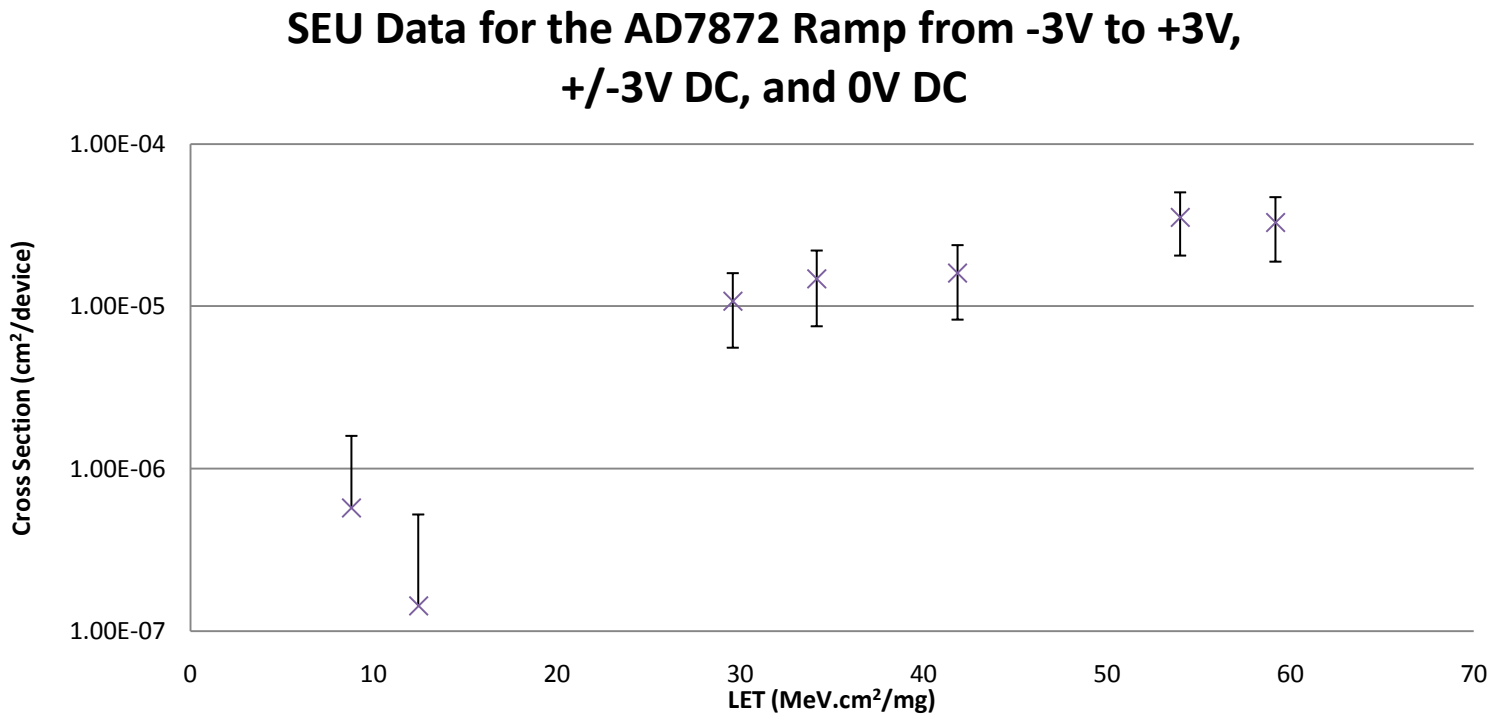


Figure 10: SEU Cross section of the 7872ARPFS device shown with +/- one standard deviation bars at each LET

## VI. Result Synopsis

Three 7872ARPFS parts were tested in the TAMU ion beam; the parts were intermittently tested for LET values of 2.8-to-59.2 (MeV.cm$^2$/mg) achieving a minimum fluence of 1 x $10^6$ (p/cm$^2$) at each LET per part, to obtain the following results:

| Occurrence: | Lowest LET where events were observed: | Highest LET where events were observed: |
|---|---|---|
| SET > 10 mV | 2.8 MeV.cm$^2$/mg | Observed at all higher LET tested (tested up to 59.2 MeV.cm$^2$/mg) |
| SEU | 8.8 MeV.cm$^2$/mg | Observed at all higher LET tested (tested up to 59.2 MeV.cm$^2$/mg) |
| Latch-up Events: | No latch-up events were observed (tested up to 59.2 MeV.cm$^2$/mg at both room temperature and >70C) | No latch-up events were observed (tested up to 59.2 MeV.cm$^2$/mg at both room temperature and >70C) |

Table 3: LET extremities of events

| Part # | Total Fluence (p/cm$^2$.s) | Total Dose (Rads) | Average Flux (p/cm$^2$.s) | Test Result |
|---|---|---|---|---|
| 1 | 2.90E7 | 2.17E4 | 2.23E4 | Still Functional |
| 2 | 2.60E7 | 4.18E3 | 2.38E4 | Still Functional |
| 3 | 3.80E7 | 1.22E4 | 2.91E4 | Still Functional |

Table 4: Results by part.

This part shows a low susceptibility to SEU independent of frequency for analog voltages between -3V and +3V on its input.

For SET the device has similar results for a changing input and a 0V throughput. As the input is held at a higher voltage the transients will have more room to “dip” allowing for them to register depending on resolution that is needed.

SEUs occurred if the strobe input line was hit or corresponding circuitry, the returned value was not read from the device at the appropriate time to contain all information. The timing diagram during a hit would have had viable voltage values not being allowed to pass through to the output with the correct timing.