



Current Spike Investigation for NAND Flash Memory

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Outline



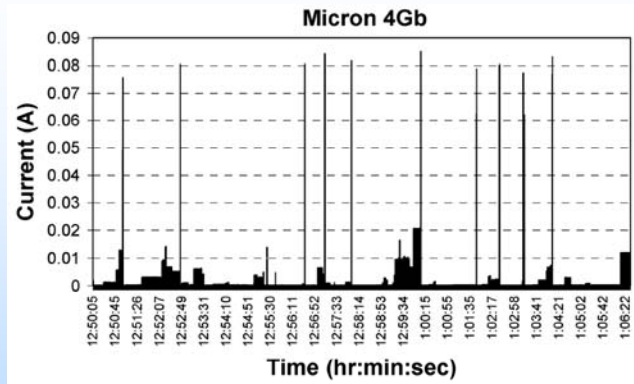
- Introduction
- Experimental Plan
- Experimental Results
- Discussion
- Conclusions

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Background

Micron 4G
Dynamic Read
 10^7 Ta ions/cm²
No failure



Irom et al., IEEE TNS, 54, 2547 (2007).

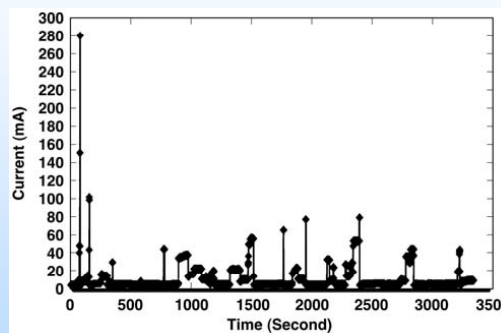
To be presented by Timothy R. Oldham at the 2011 Single Event Effects (SEE) Symposium, April 12-14, 2011, La Jolla, CA.

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Background

Samsung 8G
Dynamic Read
 10^7 Au ions/cm²
Failure



Irom et al., IEEE TNS, 57, 266 (2010).

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Calculated Event Rate In Space

- Tests were conducted with 10^7 Au ions/cm²
- Flux in GEO orbit at LET of Au is 1 particle/cm² every 7200 years
- Event rate is about 1 per 10^6 particles/cm²
- Estimated rate in space is ~1 per 7×10^9 years, assuming present conditions the whole time
- Interval is greater than age of earth, and about half interval since the Big Bang
- Even if we had duplicated these events on the ground, it would not make them real in space!

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Joint Experiment Plan

- Use parts reported to have current spikes
- Duplicate beam conditions from experiments where spikes were reported
- Use NASA LCDT, rather than alternatives
- Use three test modes: Static (with bias), Dynamic Read, R/E/W
- Test was done at TAMU using 15 MeV/nucleon tune

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Experimental Results

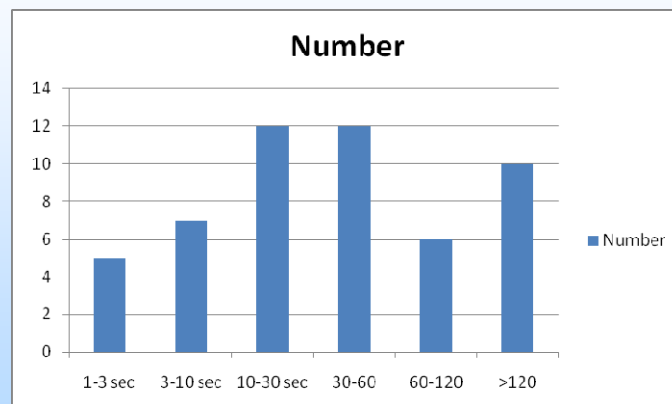
- On 38 beam runs, observed 52 high current events
- None less than 1 sec in duration, most 10's of seconds, or minutes
- 48 of 52 had stair-step structure characteristic of micro-latches
- Remaining four events appear to have been due to bus contention
- Did not observe any events 300-400 msec in duration

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Summary of Results

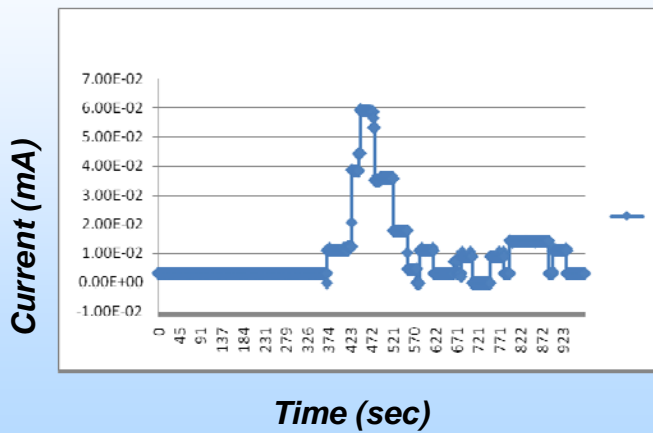


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Samsung 8G



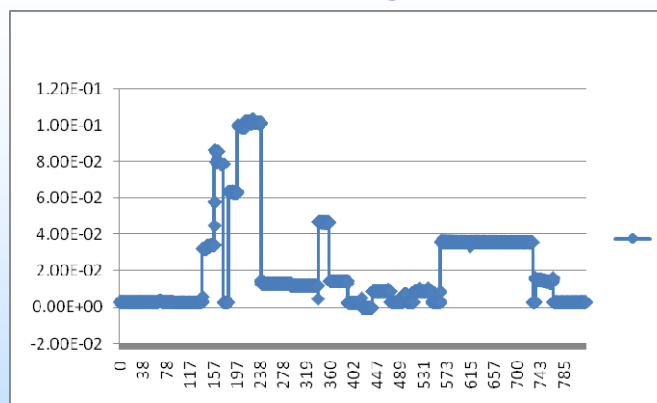
- Dynamic Read mode
- Xe ions
- No failure

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Samsung 8G



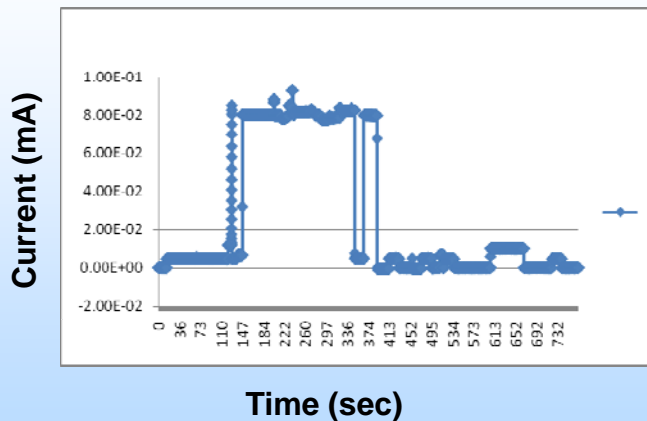
- Static mode
- Xe ions,
- Erase, write functions both failed

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Micron 4G NAND



- Xe ions
- Dynamic Read
- No failure

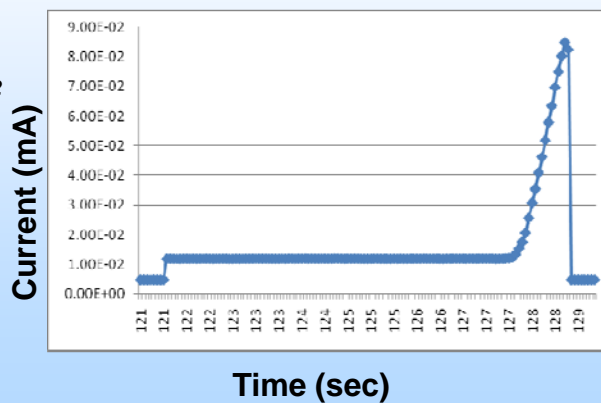
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Bus Contention

Micron 4G
Dynamic Read
 2×10^6 Xe ions/cm²
SEFI
OK after PC



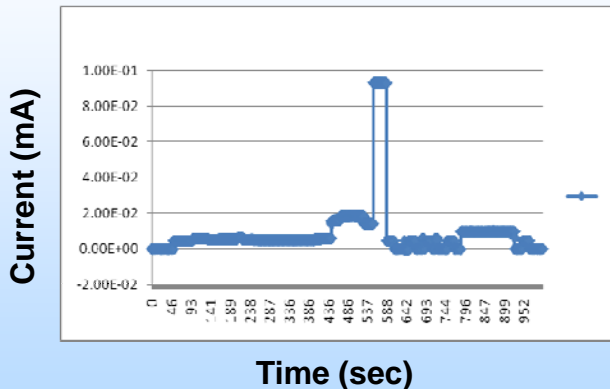
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Micron 4G NAND

Micron 4G
Au ions,
Dynamic Read
Write, Erase
both failed

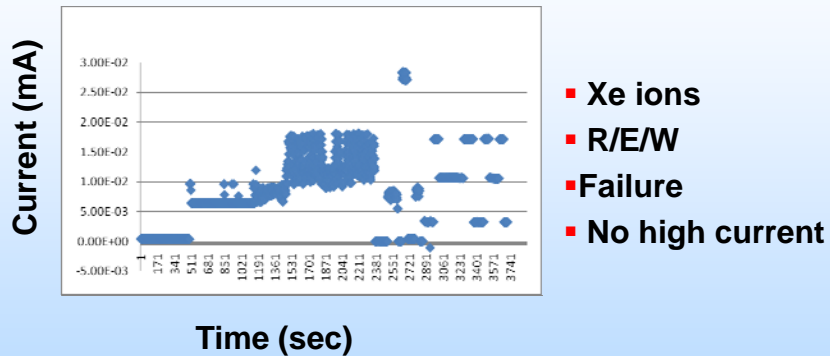


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Micron 4G NAND

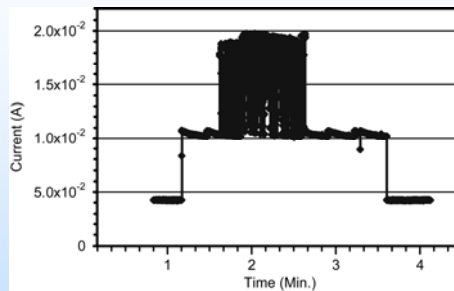


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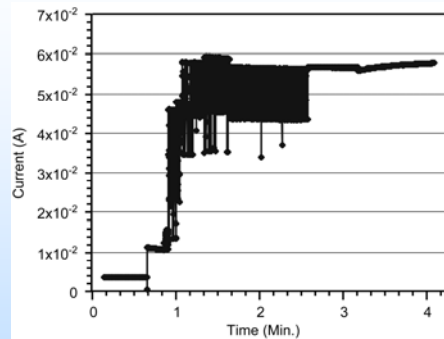
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Samsung 4G



***Xe ions, R/E/W
No Failure***



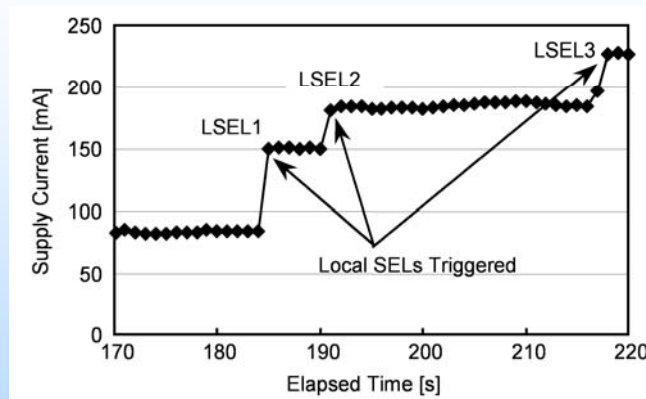
***Xe ions, R/E/W
SEGR Failure***

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Micro-Latches in Combinational Logic

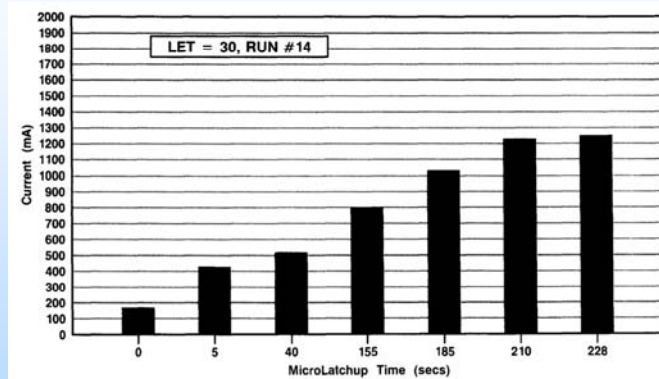


H. Shindou et al., IEEE TNS, 52, 2638 (2005).

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Micro-Latches in Intel 386 Processor

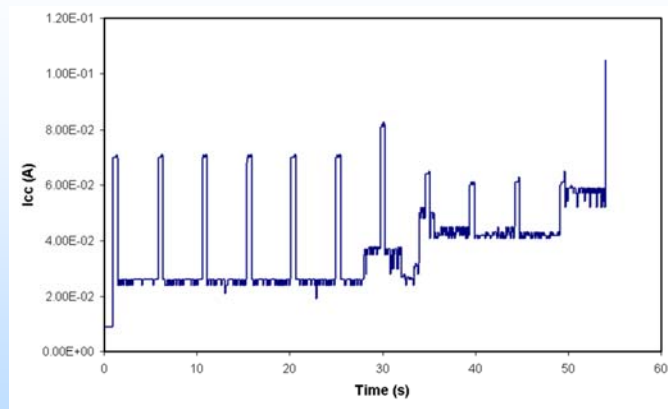


K.A. LaBel et al., IEEE REDW Record, p. 1, 1992.

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Micro-Latches in SDRAM



C. Poivey et al., 512M SDRAM Test Report
<http://radhome.gsfc.nasa.gov>

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Conclusions (I)

- **Conducted experiment designed to duplicate current spikes reported by Irom et al.**
- **Observed 52 high current events—48 LSEs (micro-latches) and 4 apparent cases of bus contention**
- **Neither bus contention nor LSEL is unique to flash memory—3 other examples cited, where test vehicle had no charge pump**
- **Showed example of failure without high current**
- **Showed examples of high current without failure**
- **Showed example where failure caused high current, not the other way around**

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Conclusions (II)

- **Even if failure and high current correlated, no proof high current caused failure**
- **Failed to duplicate “typical” 300-400 ms current spikes**
- **Four short bus contention events in 38 beam runs, not ten events in one run, and pulse widths are different**
- **Even if current spikes had been observed in ground test, rate in space would be zero**

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