National Aeronautics and Space Administration

DTRA-NEPP TECHNICAL PROGRESS REVIEW April 6, 2010

DTRA TASK TITLE:	**3.2 Test and Evaluation of the Radiation Response of Commercial and Hardened Microelectronics**
SUBTASK TITLE:	**FPGA Test and Evaluation**
DTRA TASK MANAGER:	**Ken LaBel**
SUBTASK MANAGER:	***Melanie Berg***
NON-NASA CONTRIBUTORS:	**BAE, Achronix, Actel, Xilinx, NRL**

***Note:** Not all subtask efforts are funded under this IACRO. We are reporting for interest purposes.*

KAL1

DTRA Task # (3.2) FY10: FPGAs (Continuation)

Description:

The main goal of this task is to investigate FPGAs from various vendors and to determine applicability for the space radiation environment. The following is a more detailed list of task goals.

- Determine inherent radiation sensitivities of advanced complex commercial CMOS (<100 nm) and hardened FPGAs
- Provide guidance on radiation test and qualification procedures
  - As a consultant
  - Test and analysis FPGA guideline development
- Determine SEU sensitivities for hardening approaches
- Comparison of fault injection versus beam SEU coverage
- Evaluate low proton energy sensitivity of commercial CMOS FPGAs (Low Energy test methodologies are discussed in detail in another task)

FY10 Plans:

Probable Test Vehicles:

- Achronix/BAE Hardened Asynchronous FPGA RADRunner
- Achronix Commercial Asynchronous FPGA SPD60
- Xilinx Spartan 6 (45nm SRAM-Based)
- Actel RTAX2000s FPGA (150nm Anti-fuse Based)
- Actel RT ProASIC FPGA (130nm Flash-based)
- SIRF Program support - TBD

Other Work:

- Support of Crypto space evaluation of Actel RTAX-S (90nm)
- Develop guideline for interpreting FPGA SEE data

Schedule:

- Will be presented on separate slides due to number of tasks

Deliverables:

- Test reports and quarterly reports
- Expected submissions to SEE Symposium, MAPLD, and IEEE RADECS. DTRA to review prior.

NASA and Non-NASA Organizations/Procurements:

Beam procurements: TAMU, IUCF, UC Davis,
- Possible use of Berkeley Facility

Partners:

Xilinx, BAE, Achronix, NRL, Actel

Principle Investigator: GSFC-MEI/ Melanie Berg
Other participants: GSFC-MEI/Hak Kim, Mark Friendlich, Chris Perez, Anthony Phan, Tim Irwin, Christina Seidlick

Overall Highlights - 1

- First data points on commercial 40nm Xilinx Spartan-6 devices
  - Samsung process (bulk)
  - Proton irradiation performed at Indiana last week
    - *Preliminary data shows possible decreased SEU sensitivity versus previous Xilinx technology generations*
    - *Tested dose <100krads due to FPGA being on fully populated evaluation board*
- Development of complex FPGA test circuitry
  - Enhancement to shift register testing
  - Increased observation of FPGA SEE behavior
  - Heavy Ion and Proton tests have been performed with various FPGA types and manufacturers
  - Improves characterization and subsequent error rate calculations

Overall Highlights - 2

- Renewed study of ACTEL RTAX-S (130nm bulk antifuse)
  - Embedded memory evaluation as well as internal EDAC and FIFO schemes
    - New functional interrupts (SEFI) observed not previously reported
  - complex logic function analyses
    - Revealed SEE decrease due to fanout of combinatorial logic cells
    - Demonstrates the necessity of testing beyond conventional methods (>2 orders of magnitude difference in cross sections versus simplified testing).
- Agreement in place to collaborate with Actel on RT ProASIC SEE tests

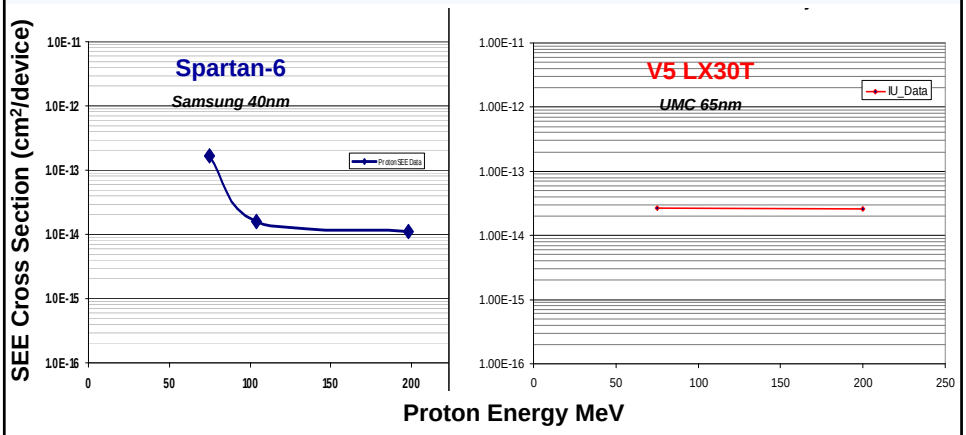
Overall Highlights - 3

- First data points on commercial 90nm Achronix SPD60
  - Partnered with NRL and their customer
  - Heavy ion (static) and proton testing (static+dynamic) performed
    - *No SEL observed*
    - *Significantly large number of configuration upsets*
  - LASER testing planned and board re-spin under discussion (noise issue) as well as follow-on heavy ion experiment
- SEE evaluation of new Radrunner from BAE/Achronix
  - Heavy ion and laser tests performed
    - Information released by BAE/Achronix
- Continued successful fault injection experiments on Xilinx Virtex-V devices

Status

Xilinx Spartan-6

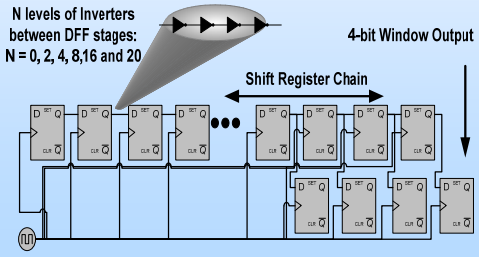
Preliminary testing: Indiana University



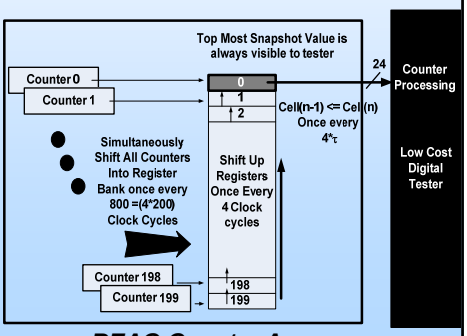
Static Configuration SEE cross section is lower at 200MeV than Previous Xilinx V5 testing

FPGA Test Structures

- Objective: develop test structures that exercise FPGA circuitry to better characterize SEE cross sections
- Windowed DFF shift register (WSR): conventional DFF tests with use of combinatorial logic
- Counters Arrays: increases complexity of test structure and introduces fanout *(novel REAG architecture)*
- WSRs and Counters are now used in all FPGA dynamic tests



REAG Windowed Shift Register String



REAG Counter Array

Goals

Actel RTAX-s

- Goal: Analysis of Embedded Memory (BRAM) Error Cross Sections
- Goal: Evaluation of design and frequency effects regarding SEE cross-sections and error rate predictions

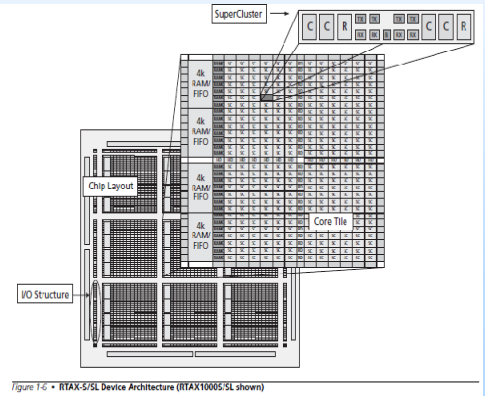
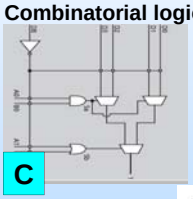


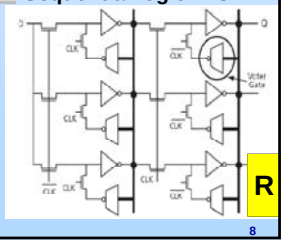
Figure 1-6 • RTAX-S/SL Device Architecture (RTAX1000S/SL shown)

Combinatorial logic C-CELL



C

Sequential logic R-CELL



R

Work Plan

Actel RTAX-s Designs Under Test : Memory

- **Develop Actel RTAX-s Embedded Memory Designs:**
  - **memory control (Address counters + memory enables)**
  - **Embedded memory blocks (with and without EDAC+FIFO)**
- **Functional Logic Designs Under Test:**
  - **Six WSR strings with various levels of combinatorial logic.**
  - **Counters Arrays: 200 Counters.**
- **Develop Test Vehicle using High Speed Digital Tester (HSDT)**
- **Paper Submission to RADECS (counter logic specific):**

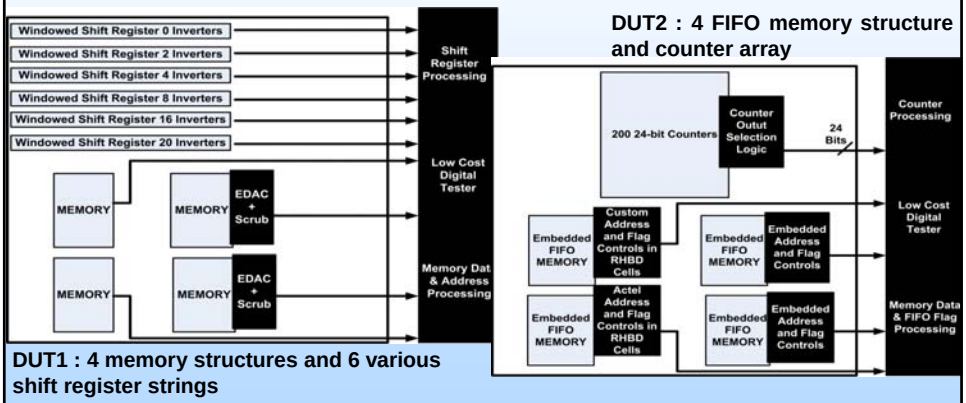
"SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices"

- **Single Event Effects Symposium Presentation 04/2010**

STATUS:

Actel RTAX-s

- **RTAX-s Heavy Ion Testing December 2009**
- **RTAX-s preliminary test report delivered 02/2010**

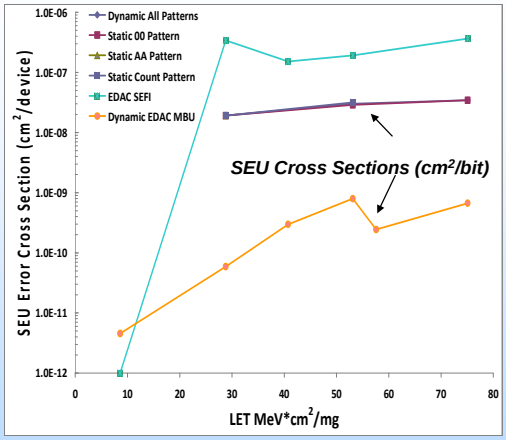


DUT1 : 4 memory structures and 6 various shift register strings

RTAX-s Design and Tester were successfully completed within 2 months

Highlights:

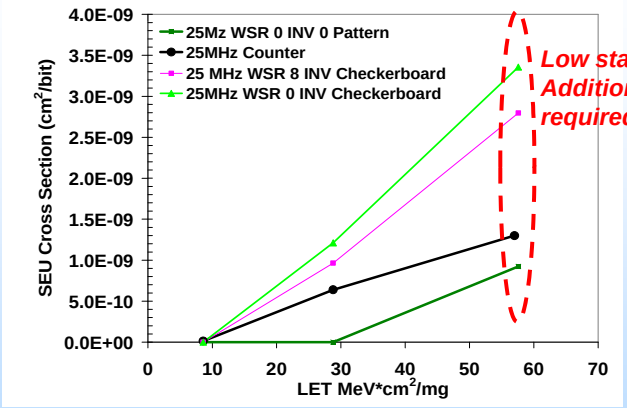
Actel RTAX-s Static Embedded Memory Results



EDAC improved BRAM SEE cross Sections by > 2 orders of magnitude (until SEFI)

Highlights

Actel RTAX-s : Counters versus WSRs



Data Pattern and capacitive loading significantly affects LET_{th}

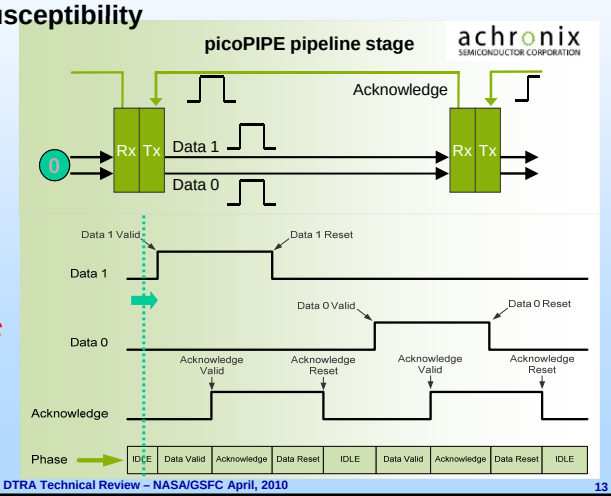
Design/Data Pattern	8 Inverter/ Checker	0 Inverter/ Checker	0 Inverter/ 0 pattern	Counter
LET_{th} MeV*cm²/mg	>8	>8	>30	>8

Goals:

Achronix SPD60

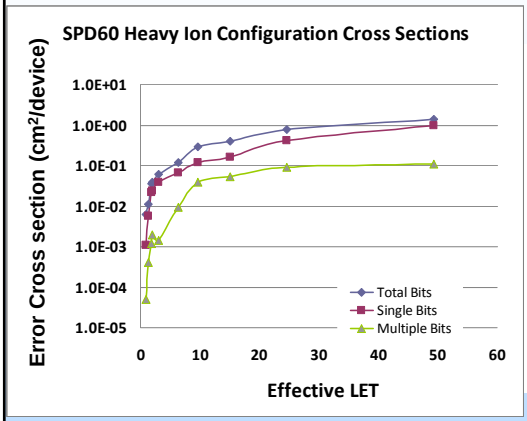
- **Achronix SPD60 is a SRAM-Based FPGA with Asynchronous data flow.**
  - **Configuration susceptibility**
  - **Functional logic susceptibility**

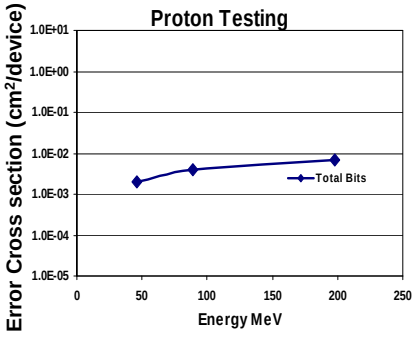
Asynchronous Logic Fabric



STATUS

Achronix SPD60



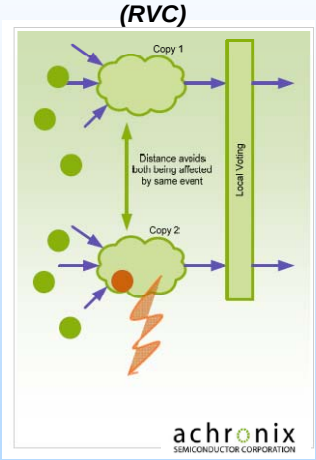


Significant number of multiple bit upset… data is further being analyzed

Goals and Work Plan:
Achronix/BAE RADRUNNER

- **RADRUNNER is a hardened SRAM-Based FPGA.**
  - **Configuration:**
    - **Rad Hard 150 nm CMOS Technology (RH15) from BAE Systems**
    - **Total-dose tolerance greater than 1 Mrad**
    - **Upset rate of less than $1E^{-12}$ upsets/bit-day**
  - **Functional logic**
    - **Based on Achronix SPD60**
    - **Includes Redundancy Voting Circuits (RVC)**
    - **All paths are duplicated**
- **Tests encompass configuration and functional logic evaluation:**
  - **Configuration Readback**
  - **WSRs and counter arrays**

Redundancy Voting Circuit (RVC)



Status:
Achronix/BAE RADRUNNER

- **Heavy Ion Tests were performed at TAMU Cyclotron in February 2010.**
  - **Functional logic LET_{th} > 3 MeV*cm^2/mg (currently under analysis)**
  - **Configuration did not upset**
  - **No Single Event Latch-up Observed (SEL)**
- **Laser testing March 2010 included:**
  - **Configuration susceptibility**
  - **Functional logic susceptibility**

PLANS FOR FY10

- **Actel RTAX-s**
  - **Technical plans**
    - **May or June 2010 Heavy Ion Testing**
    - **Hone in on LET_{th} of the WSRs, counters, and memory modules**
  - **Deliverable plans**
    - **Update and release current Test Report (July 2010)**
    - **RADECs paper submission (04/01/2010)**
    - **SEE presentation (04/2010)**
- **Actel RT ProASIC (Flash Based FPGA configuration)**
  - **Technical plans**
    - **Heavy Ion and Proton Testing end of FY10**
    - **WSRs, counters, and memory modules (similar to RTAX-s)**
  - **Deliverable plans**
    - **Currently in discussion**

PLANS FOR FY10

- **Xilinx Configuration-Hardened SIRF**
  - **Technical plans**
    - **Heavy Ion and Proton Testing end of FY10**
    - **WSRs, counters, and memory modules (similar to RTAX-s)**
  - **Deliverable plans**
    - **Currently in discussion**
- **Xilinx Spartan 6**
  - **Technical plans**
    - **Heavy Ion and low energy Proton Testing end of FY10**
    - **WSRs and counters with and without mitigation**
  - **Deliverable plans**
    - **Indiana University -Proton Test Report 04/2010**

PLANS FOR FY10

- **Achronix SPD60**
  - **Technical plans**
    - **Laser Testing 5/2010**
    - **Further Heavy Ion Testing end of FY10**
    - **WSRs and counters**
  - **Deliverable plans**
    - **Test Report 05/2010**

SCHEDULE

	Microelectronics T&E	2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
Actel RTAX-s	On-going discussions for test samples												
	Radiation Test Development and Testing												
	Data Evaluation and Test reports												
	Paper Submission												

TBD waiting for Vendor DUT design

Schedule

	Microelectronics T&E	2009 O	N	D	2010 J	F	M	A	M	J	J	A	S
BAE/ Achronix FPGA	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

Schedule

	Microelectronics T&E	2009 O	N	D	2010 J	F	M	A	M	J	J	A	S
Achronix FPGA	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

Schedule

	Microelectronics T&E	2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
Spartan6	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

Schedule

	Microelectronics T&E	2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
Actel ProASIC	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												