ADC/DAC test techniques

Introduction

There is a general need for spacecraft systems to make use of advances in analog to digital (ADC) and digital to analog (DAC) technologies. In particular, imaging systems such as star trackers and remote sensing instruments require 14,16, or more bits ADCs that have low power consumption, fast conversion rates (>1 MSPS) and good radiation tolerances.
Because ADC and DAC have both analog and digital functions, they are mixed-signal devices. Most of state of the art ADC/DACs are processed in CMOS technologies. Therefore, the two radiation issues are total ionizing dose (TID) and Single Event Effects (SEE). Because of the accuracy needed to perform analog to digital or digital to analog conversions, a small degradation of one of the device elements can have a significant impact of the overall device performance. For example, internal voltage reference degradations impact significantly the performances of ADCs [1 Layton dw 03]. Available data show that all ADC/DAC have a low to moderate tolerance to TID [1, 2 **Bings dw03**, 3 Hopkinson dw00, 4 Black dw98, 5 LTC1657 report, 6 AD7714 report]. ADC and DAC are also very sensitive to SEEs: Single Event Transients (SET) in the analog part and Single Event Upsets (SEU) in the digital part. SETs generally cause small deviations in the device output [7 Turf tns90, 8 Turf tns94], and SEUs may cause large variations of the device output. Lingering errors or Single Event Functional Interrupts (SEFI) were also observed [9 Bee Radecs97, 10 Bee dw98, 11 AD7714 report, 12 Wilson dw94]. The SEU/SET LET thresholds are generally low, below 5 MeVcm2/mg, and proton induced SEU/SET were observed [8 Turf tns94].
Converters are complex devices with different architectures. Each converter type has its specific vulnerabilities.
The objective of this document is to survey the existing ADC/ DAC radiation test methods. One of the main challenges of testing high resolution ADCs, DAC is the accuracy of measurements. For example, for a 5 V input range 16 bit ADC, the least significant bit, LSB, represents a variation of the input voltage of about 75 µV.

Reminders, ADC performances

An ADC is a device that provides an output that digitally represents the input voltage or current level. An ADC has an analog reference voltage or current against which the analog input is compared. The input/output transfer function is given by the following formula:

$$Output = 2^n \times G \times A_{IN} / V_{REF}$$

- n = number of output bits (resolution)
- G = gain factor (usually “1”)
- A_{IN} = analog input voltage (or current)
- V_{REF} = reference voltage (or current)

Fig 1 is a conceptual drawing showing the operations of an ADC. The device transfer curve indicates how well the ADC performs. It should be noted that most devices have sufficient noise, the quantization noise, that a given input voltage will be converted into a range of digital readings covering 2, 3, or even more adjacent values. Therefore, the transfer curve is obtained by averaging techniques.
Several parameters can be extracted from the conversion curve. First, a best fit line can be calculated. The best fit line is a straight line between the points defined by the first and last code transitions. The average gain and offset of the line can be compared to an ideal curve. Deviations of the transfer curve to the best fit line are very important and are generally given as Differential Non Linearity (DNL) and Integral Non Linearity (INL). DNL is the difference between the ideal and the actual input code width. INL is the maximum deviation of the transfer function from the best fit line.

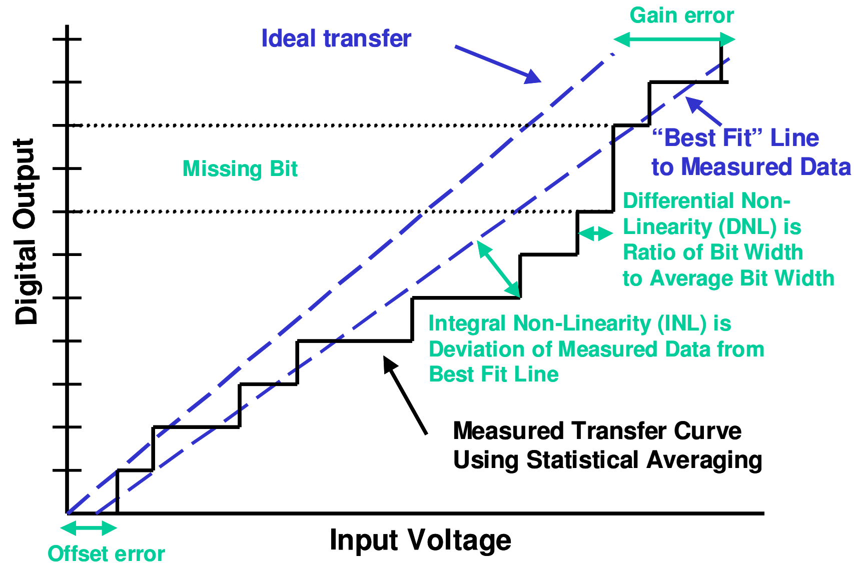

Fig 1: Basic (DC) functionality of ADCs [13 Tausch, short course 2000]

Other key parameters come from the time domain response of the ADC. Internal analog circuitry of the ADC may not respond to a large step input as quickly as desired. It may take several conversions before a reading is stable to the desired resolution. This time is defined as the settling time.
A third set of parameters is associated with the frequency response. To do this, a sinewave is digitized with the ADC and recorded in a sequential data file. Then, this file is analyzed using Fast Fourier Transform (FFT) techniques to generate the frequency domain representation of the data. Figure 2 shows a typical representation of the FFT data in term of decibels (dB) versus the frequency.

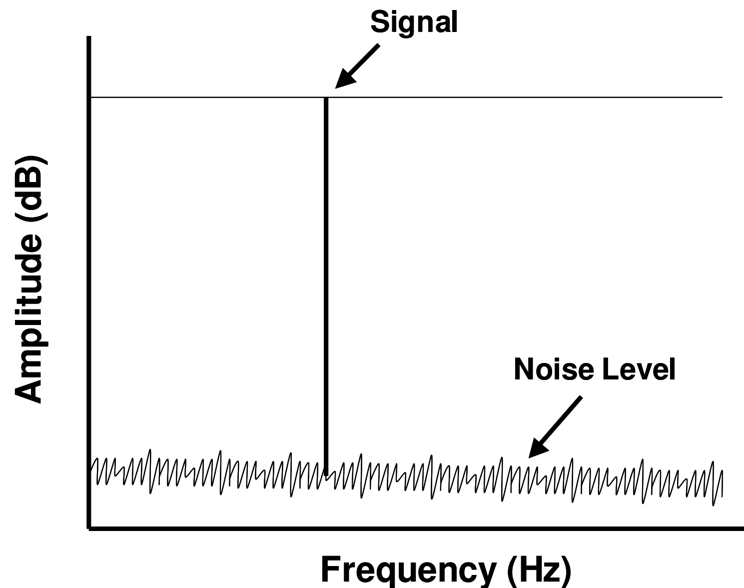

Fig 2: typical frequency domain representation

Once the FFT calculation is done, parameters such as signal to noise ratio (SNR), total harmonic distortion (THD), signal to noise and distortion (SINAD), and effective number of bits (ENOB) can be calculated.:

- SNR is the ratio of the output signal to the output noise level not including harmonics or DC.
- THD is the ratio of the root mean square (rms) total of the first six harmonic components to the rms value of the output signal and relates the rms sum of the amplitudes of the harmonics to the amplitude of the fundamental.
- SINAD is a combination of the SNR and the THD. It is defined as the rms value of the output signal to the rms value of all the other spectral components below half the clock frequency, including harmonics but excluding dc. Because SINAD compares all undesired frequency components with the input frequency, it is an overall measure of ADC dynamic performance.
- ENOB is a specification that helps to quantify dynamic performance. ENOB says that the converter performs as it were a theoretically perfect converter with a resolution of ENOB. That is, an ENOB of 7.5 bits says that converter performs, as far as SINAD is concerned, as if it were an ideal 7.5 bit ADC.

In an ADC, noise comes from three sources:

- quantization noise: it results from the quantization process, the process of assigning output codes to input ranges. The amplitude of the quantization noise decreases as resolution increases.
- noise generated by the converter itself.
- application circuit noise.

TID testing

Introduction

Available data show that as converter designs have evolved to increase resolution, speed, and accuracy, their radiation tolerance has diminished [14 Lee tns 95, 5 **Crane1657 report**]. The reason for the decreased tolerance appears to be related to the increased complexity of internal circuitry that is needed to increase performance and accuracy, not fundamental differences in the radiation response of internal components. For example, some devices use an internal microprocessor and error registers to provide self calibration or first order inaccuracies. These devices are the most sensitive to total dose degradation [14 Lee tns 95, 6 NAVSEA 7714 report].

Figures 3, 4, 5, 6, 7, and 8 are oscilloscope pictures of the output of on the 16 bit DAC LTC1657, at pre-rad, 5krad(Si), 7.5krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si) respectively [5 crane1657 report]. Applying an input vector to the device from 0000h to FFFFh created these plots. This created a corresponding ramp on the output of the DAC. These plots visually show how much degradation is occurring as dose levels increase. We can see code weighted errors starting at 5 krad(Si) that will lead to large INL/DNL errors. Then, at higher dose levels, we can see large discontinuities corresponding to loss of major code transitions. After 20 krad(Si) the part is not longer working properly.

Figure 12-LTC1657 transfer curve Pre-Rad

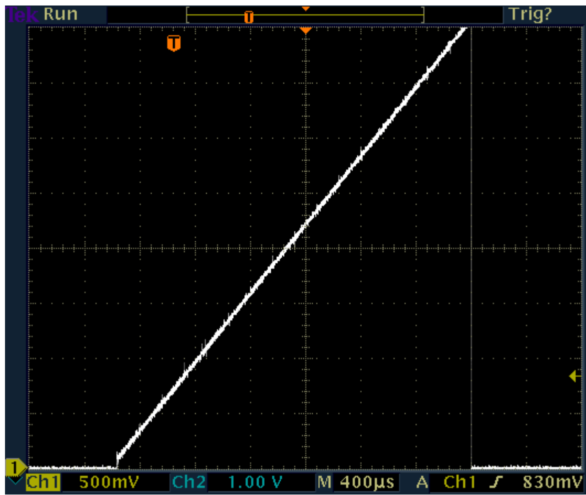

Figure 13-LTC1657 transfer curve after 5krad(Si)

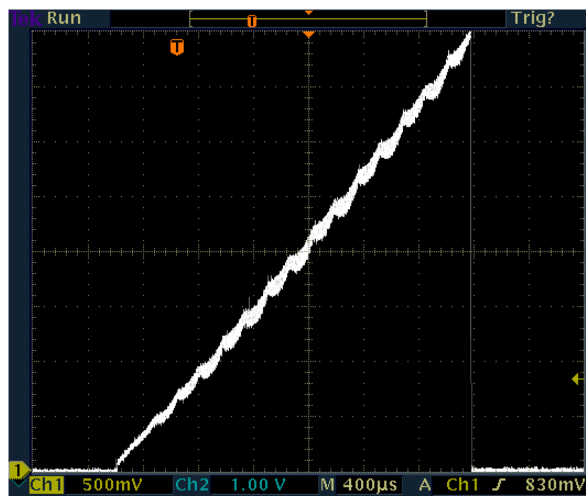

Figure 14- LTC1657 transfer curve after 7.5krad(Si

Figure 15-LTC1657 transfer curve after 10krad(Si)

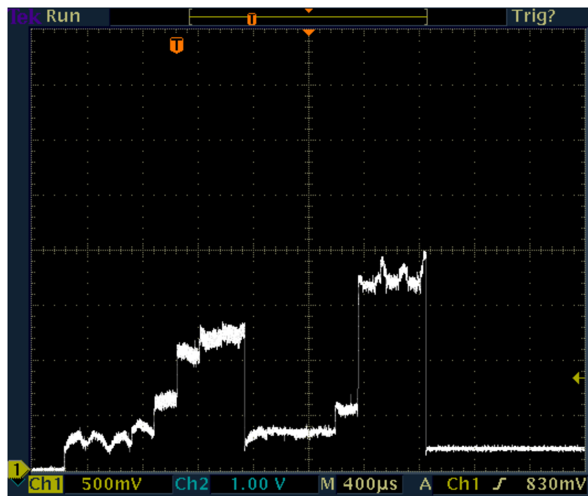

Figure 16-LTC1657 transfer curve after 20krad(Si)

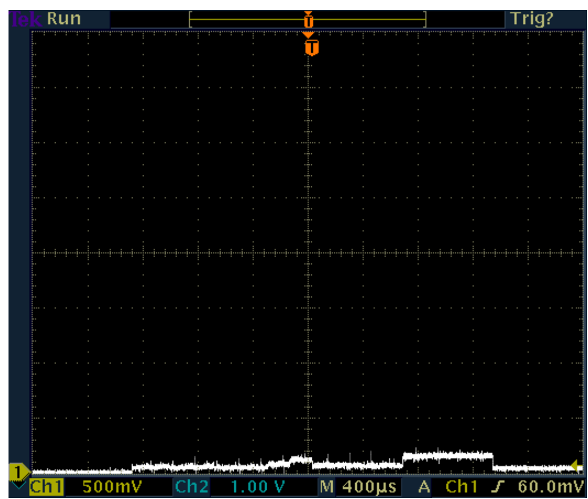

Figure 17-LTC1657 transfer curve after 30krad(Si)

Irradiation conditions

Most ADCs are processed in CMOS or BiCMOS technology. On could expect that most devices will survive much higher radiation level at low dose rate. Therefore, there is an advantage to test CMOS devices at the lowest dose rate that is practically possible. However, data show examples of increased degradation at very low dose rate [14 Lee tns95]. Therefore, it is very critical to perform the high temperature annealing after irradiation. Data show several cases of rebound after annealing [14 Lee tns95] or increased degradation after annealing [3 Hopkinson dw00].

Bias conditions during irradiation

Available TID test data show the importance of specifying bias conditions to match actual operating modes:

- Static bias and dynamic bias can give totally different part response to radiation. However, clock is not the only parameter. AD9220 data [15 turf dw96] show the strong effect of the input bias. Parts exposed with a static input degrade significantly more than parts exposed with a dynamic input. A static input bias resembles systems control sensor applications, but in applications where the input is changing constantly a test with a static bias input will underestimate the part tolerance
- Test data on the 16 bit ADC CS5016 [14 lee tns 95] show that the use an external clock, instead of the device internal clock, can not only improve the device operational functionality but also improve the radiation failure level of devices.

Electrical measurements, test set-up

In addition to parametric tests, it is important to check the converter functionally. This must be done over the entire voltage range because some failure modes may affect the linearity and range only near the extremes of the specified input range.

Such parameters as Icc, Ioz, Vref, and Voh/Vol along with a static functional test can be easily set up and measured with a digital test system with a precise analog signal source. On the other hand, tremendous effort is required in order to test a high resolution and high-speed ADC for full specifications:

- A histogram test is required for the dynamic linearity test.
- A FFT test set-up for SNR measurement is very difficult and noise is the major problem. This dynamic test set-up not only requires delicate equipment and expensive precision test systems but also requires time consuming preparation.

Linearity testing: to perform linearity testing, it is necessary to collect a large number of measurement samples over the full input voltage range. Generally a spectrally pure sinewave is applied at the input of the converter and the output samples are stored for further statistical analysis. A code with more or less occurrences than average appears as a DNL greater or less than zero LSB. Fig 3 shows an example of INL degradation versus dose.

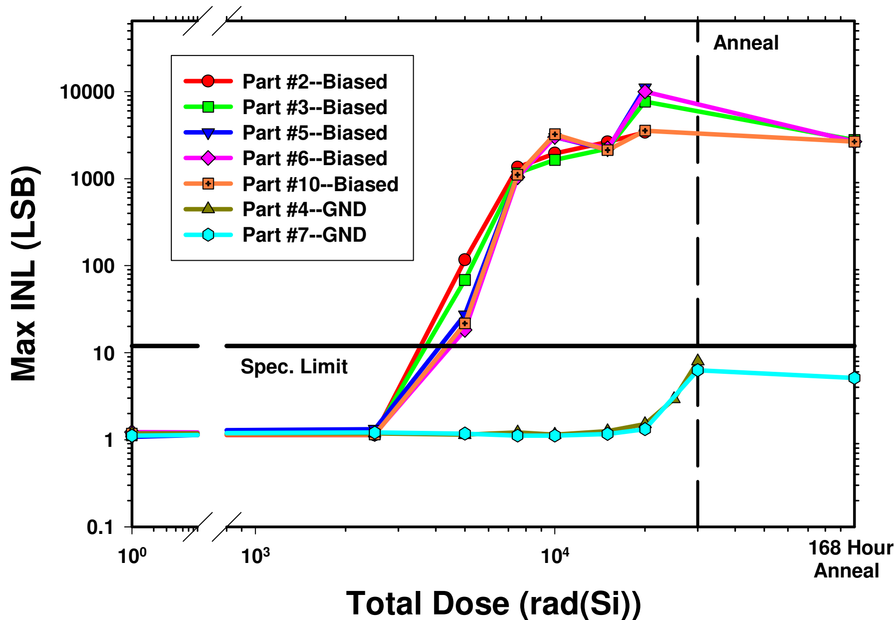

Fig 3: Degradation of LTC1657 16 bit DAC INL versus dose [5 Crane 1657 report]

Power supply current: Although linearity errors are important characterization parameters, power supply current can be an effective indicator of global degradation of either the subthreshold leakage of internal CMOS transistors, or field oxide leakage. Fig 4 shows an example of large degradation of power supply current versus dose.

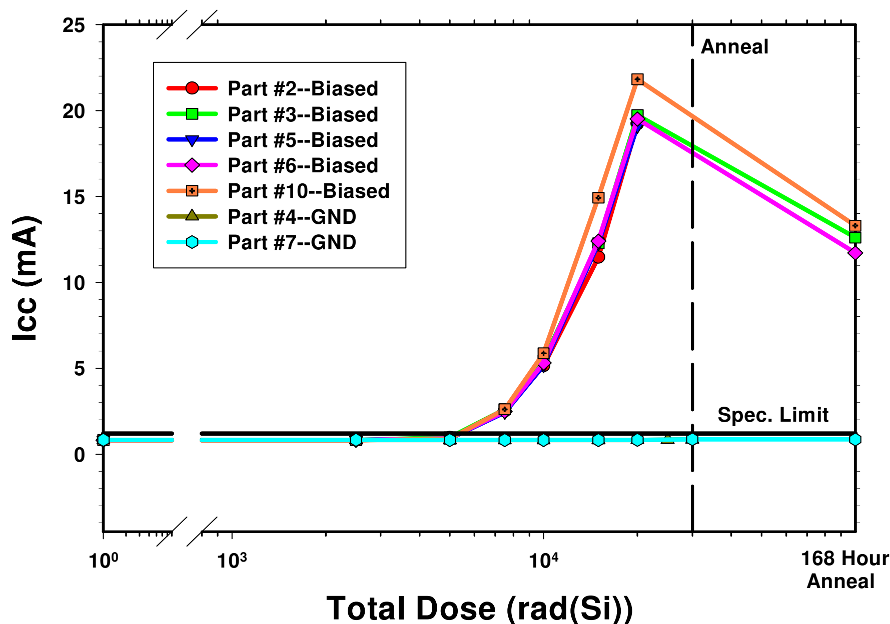

Fig 4: Degradation of Icc versus dose, LTC1657 16 bit DAC [5 Crane1657 report]

Reference voltage testing: The reference voltage is one of the most critical parameters because the reference voltage establishes the gain required to meet the highly accurate specifications of these converters. Even though some ADCs use external voltage references, changes in the reference internal buffer circuitry will affect the reference voltage at internal points within the circuit.

FFT testing: FFT techniques are very useful to show the increase of the noise floor level. Some products uses an internal clock, this clock degrades with radiation. Any noise or disturbance in the clock will induce conversion errors. Therefore, it may be impossible to perform the FFT tests with the internal clock, and it may be necessary to use an external clock [14 Lee tns95].

SEE testing

Introduction

When an energetic heavy ion or proton strikes an ADC or a DAC, three different kinds of errors can occur:

- Single Event Transients (SET) in the analog part of the device or Single Event Upsets (SEU) in the device's digital latches. Both analog and digital disturbances will be recorded as an erroneous output during a conversion cycle. If the analog signal path is disturbed, the errors may be clustered around the expected value. If latches are upset, errors with large numeric offsets from the expected value may occur [16 Turf tns 89].
- Lingering errors: an erroneous output is observed at the device output during several consecutive conversion cycles. In some cases, a lingering error may be a Single Event Functional Interrupt (SEFI). The device does no longer work properly, and a reset is necessary to restore functionality.
- Single Event Latchup: Ahigh current condition occurs in a parasitic SCR structure of CMOS devices. SEL events may be destructive. A power cycle is necessary to recover from a SEL condition.

Irradiation conditions

ADC/DAC are very sensitive to SEE. They are generally sensitive to both heavy ions and protons induced events. We recommend performing heavy ion and proton SEE tests on these devices. It is important to use a flux that is low enough to capture all the events. Data show that ADC/DAC exhibit several error signatures [7 Turf tns 90, 8 Turf tns94, 17 Buchner tns00, 18 Heidergott tns01]. It is necessary to capture a large number of events to get statistically significant results.

Bias conditions

Parts under tests are continuously performing AD or DA conversions. The conversion rate has an impact on sensitivity, especially on the SET induced errors. We recommend to test the device at the maximum conversion rate or at the application conversion rate.
The analog input voltage has also an impact on the device sensitivity. Data [17 Buchner 00, 19 Buchner radecs03] show that the spatial distribution of SEU as well as the SEU cross section depends on the analog input voltage. Device SEU sensitivity may vary by more than order of magnitude with the input voltage. It is therefore important to test the device for all the input range. However, input signal waveform can be different of the actual application in terms of frequency without any impact on the SEE results. Input signal selection is often dictated by test set-up constraints as will be detailed in the next section.

Electrical measurements, test set-up

SELs are detected by monitoring the device under test (DUT) power supply current. Other events are detected by monitoring the DUT output when the device continuously performs AD or DA conversion. The detection of single event errors is very challenging. Single event errors occur relatively infrequently within a continuous flow of measurements. The volume of data corresponding to an irradiation run is enormous. For example an ADC with a 10 million sample per second (MSPS) conversion rate will generate one billion data point during a 100 seconds exposure. It is therefore important to perform the error detection in real time.

The two traditional methods used for SEE test of ADC/DAC use two converters:

- the DUT is in series with the complementary device, DAC + ADC or ADC + DAC. This approach allows processing the data either with a numerical approach or, on the contrary, as analog signals.
- The golden chip test method: The same input is applied to the device under test and a reference device, the golden chip, and the output of the two devices is compared.

These two approaches present the advantage that they allow an easy detection of errors even with a dynamic input signal that exercises all the DUT input range. These two approaches require an initial calibration phase as the two devices, DUT and complementary or DUT and golden chip, may have different gain and offset errors. The disadvantage of these methods is that the noise of the complementary device or golden device is added to the noise of the DUT. The non-linearity errors are added as well. For 14 to 16 bits devices, it is common to get 1 or 2 LSB of instability because of the quantization noise and the differential non-linearity errors. With two devices we get 2 to 4 bits of instability. Therefore, for a 16 bit converter, it is only possible to test 12 out of the device's 16 bits.
One solution to get a better accuracy is to apply a clean DC input voltage on the DUT. The digital output is stable, and can be stored as a reference. This reference is then compared to the device output during irradiation. The disadvantage of this method is that the part is tested for only one input voltage at one time, and the test should be repeated for several input values covering the whole device input range. For example, with this set-up and using the manufacturer evaluation board, we have been able to test 14 bits of the 18 effective bits of the AD7714 [11 AD7714 test report]. The AD7714 AD converter has a 2.5V input range, this corresponds to one LSB of about 9 µV.
Another interesting method that minimizes the number of bits that cannot be observed and also overcomes the static input disadvantage is based on differential detection [20 ADS8321 test report Hirex]. It consists in comparing the DUT output signal with its own average value. This requires that the input signal changes slowly and that the transitions corresponding to SEU errors are short. With this method the effects of static gain and offset errors are automatically compensated. The disadvantage of this method is that it requires a complex set-up to obtain in real time output average value. This is done by integrating the DUT output taking into account the input signal slope.

Whatever the SEU error detection set-up, lingering errors are detected when several consecutive errors are detected. When this happens a lingering error is counter, and the device is reset.

The raw error data collected during irradiation runs need then to be analyzed to establish the different error signatures. On ADC, DAC we generally distinguish two different types of errors [7 Turf tns90]:

- small magnitude errors, that may be considered as a heavy ion induced noise component with a gaussian distribution around the nominal DUT value.
- large magnitude errors that are randomly distributed in the whole DUT output range.

This analysis can be done a posteriori or in real time with different counters for small and large magnitude errors.

References

[1] P. Layton & al, "TID performance Degradation of high precision, 16-bit Analog-to-Digital Converters," IEEE NSREC 2003 Data Workshop Records, p 6-10.
TID data paper on 3 ADCS (CS5016, 7805, 7809), mention measurements problems and the impact of Vref on INL and DNL, test on LTS2020, TNT and bench (SINAD)

[2] J. Bings, "Total Dose Results for the AD9225RH Analog-to-Digital Converter," IEEE NSREC 2003 Data Workshop Records, p 38-42.
Just TID data on AD9225RH with NAVSEA Burr Brown test system using a AD evaluation board

[3] G. Hopkinson, "Radiation Evaluation of Low Power CMOS 12 bit ADCs," IEEE NSREC 2000 Data Workshop Records, p 74-79.
TID and SEL data on AD9223 and LTC1415, just data (good introduction)

[4] J. Black, "Total Dose Evaluation of State of the Art Commercial, Analog to Digital Converters for Space-Based Imaging, Applications," IEEE NSREC 1998 Data Workshop Records, p 121-126.

TID data on 11 10 to 14 bits ADCS (AD9200, HI5746, SPT7855, XRD64L15, AD9042,…). Only two parameter tested (Icc and DNL), basic data

[5] LTC1657 test report TID

[6] AD7714 test report TID

[7] T. Turflinger & al., "Understanding Single Event Phenomena in Complex Analog and Digital Integrated Circuits," *IEEE Trans. Nucl. Sci*., vol. 37, pp. 1832-1838, Dec. 1990.

Sep ANALYSIS – ERROR SIGNATURES ON adc, offset and noise errors

[8] T. Turflinger & al., "Single Event Effects in Analog to Digital Converters: Device Performance and System Impact," *IEEE Trans. Nucl. Sci*., vol. 41, pp. 2187-2194, Dec. 1994.

[9] S. Bee, "Measurements of SEE in ADCs," ," RADECS 1997 Data Workshop Records, p 81-88.
Cf252 SEE data on AD676, AD7884, and AD7893. Good description of test methods, shows differences between agile and static inputs, shows lingering errors.

[10] S. Bee, "Heavy-ion Study of Single Event Effects in 12- and 16-Bit ADCs," IEEE NSREC 1998 Data Workshop Records, p 58-67.
SEE data on AD676, AD7884, AD78393, different results obtained with a static and an agile input, very few details on test setup (see RADECS97 paper from same author)

[11] "Heavy ion single event effect test of 24 bits ADC AD7714 from Analog Devices, test report, NASA-GSFC, March 2002.

[12] D. Wilson, "Characterization of Single Event Effects for the AD677, 16-bit A/D Converter," ," IEEE NSREC data workshop 1994 Data Workshop Records, p 78-85.
SEE data on AD677. Shows transient and lingering errors, and with an agile input signal shows gain and offset errors. They used an evaluation board.

[13] J. Tausch, "Radiation Testing of Mixed-Signal Microelectronics," IEEE NSREC 2000 short course proceedings, July 2000.

[14] C.I. Lee, "Hardness assurance and Testing Technoques for High Resolution (12 to 16 bits) Analog-to-Digital Converters," *IEEE Trans. Nucl. Sci*., vol. 42-6, pp. 1681-1688, Dec. 1995.
Comprehensive TID data on CS5016, AD7872, and MX674. Interesting considerations about testing. the author claims that static testing may be sufficient.
See ref: S Pei and SP Chan, "New Approach to Linearity Testing of ADC," Int J Electronics, 1991, vol 70, n 6, 1049-1062.

[15] T. Turflinger, "Radiation Effects in Analog CMOS ADCs," IEEE NSREC 1996 Data Workshop Records, p 6-12.
TID data on AD9220 abd AD7874. Shows the difference between agile and static inputs (makes a good point: a lot of actual applications have a static input [system control sensors]). Extensive testing but no description of test method. For this, refer to a NSREC89 presentation from the same author.

[16] T. Turflinger, "Transient Radiation Test Techniques for High-Speed Analog to Digital Converters," *IEEE Trans. Nucl. Sci*., vol. 36, pp. 2356-2361, Dec. 1989.

[17] S. Buchner, "Characterization of SEU in a flash ADC (AD9058)," *IEEE Trans. Nucl. Sci*., vol. 47, pp. 2358-2364, Dec. 2000.
Flight, Heavy ion and laser data. Shows that the main contributor to SEU are the input voltage comparators and that only a limited number of SEU signatures can happen depending on the input voltage. The sensitivity varies strongly with the input voltage. No effect of test frequency on results (this part is not very convincing)

[18] W. Heidergott, "Complex SEU Signatures in High-Speed Analog to Digital Conversion," *IEEE Trans. Nucl. Sci*., vol. 48, pp. 1828-1832, Dec. 2001.
SEE data on MAX108, shows the effect of frequency and input value, and shows the variety of SEE signatures.

[19] S. Buchner & al., "Validity of Using a Fixed Analog Input for Evaluating the SEU Sensitivity of a Flash Analog-to-Digital Converter," presented at RADECS 2003.

[20] "Heavy ion radiation test report, ADS8321 16 bit high speed, Analog to digital converter from Burr Brown," Hirex, May 2000.

S. Aghara&al., “Degradation of Commercially Available DAC ICs in a mixed-Radiation Environment,” IEEE NSREC 2003 Data Workshop Records, p 34-37.

Gamma-neutron data on a 8 bits ADC MC1408, just data, test on a Teradyne A567

L Scheick, “SEE Evaluation of Digital Analog Converters for Space Applications,” IEEE NSREC 2001 Data Workshop Records, p 62-66.

SEE data on 4 DACs (AD768, AD8420, MAX539, X9C503, just data, very short description of test set up (golden chip method?). Xicor part sensitive to SEL

G. Youk, “Dose Rate Effects of a Bipolar A/D Converter,” IEEE NSREC 1996 Data Workshop Records, p 38-43.

Basic TID data on AD574 (high dose rate testing)

A.S. Artomonov, “ADC/DAC Radiation test Technique,” RADECS 1997 Data Workshop Records, p 56-60.

TID and Dose rate data on 2 ADCs and DAC. Talk a little bit about test techniques