Anatomy of an In-flight Anomaly: Investigation of Proton-Induced SEE Test Results for Stacked IBM DRAMs

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Abstract

We present ground test and space flight data describing a single event anomaly that affects multiple bytes in a stacked DRAM module. A 12 Gbit solid state recorder containing 1,440 DRAM die experiences the anomalous events at a rate requiring testing of a large sample set of these modules.

I. Background of Anomaly

A solid state recorder (SSR) containing 12 Gbits of memory for telemetry storage was installed on the Hubble Space Telescope (HST) in February of 1997. The HST is in a 600 km circular orbit at an inclination of 29°. The orbit makes several passes through regions of high energy protons trapped in the South Atlantic Anomaly (SAA) every day. There are also low levels of heavy ions from galactic cosmic rays and solar events (see Figure 1). The maximum linear transfer (LET) of the galactic cosmic rays is approximately 20 MeV-cm^2/mg. During solar events, particles with LETs up to 100 MeV-cm^2/mg. can reach the HST orbit. Although this environment is considered benign when compared to other orbits, the HST program has learned that it must nonetheless be evaluated for radiation effects.

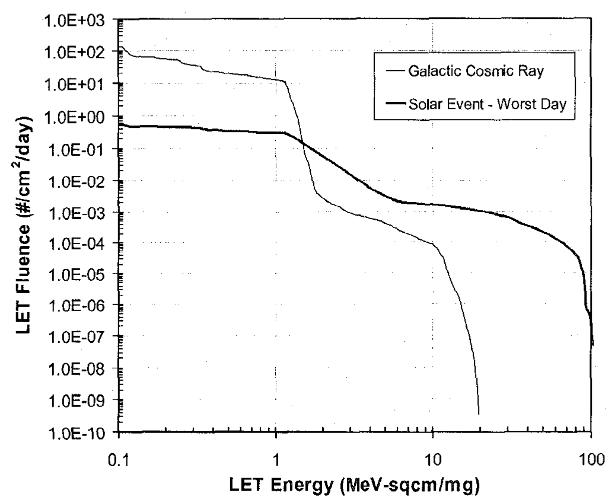

Figure 1: Total integral LET spectra for elements 1 through 92 in silicon. HST circular orbit with inclination 29 degrees and 600 km altitude. Peak solar minimum conditions and 100 mils aluminum shielding (CREME96).

A. Description of Solid State Recorder

The large memory in HST's SSR required the usage of 1440 16 Mbit dynamic random access memory (DRAM) devices. The IBM die (part number, Luna ES Rev. C - DD3 die process*) are configured as individual nibbles (i.e., 4Mx4 per die) and operate on a 5.0 V power supply. They are packaged into 320 Mbit modules (20 active die) for space flight by Irvine Sensors Corporation (ISC). The modules actually contain two stacks: each with ten active die plus two "cold" redundant die. Figure 2 is a photograph of one of the ground irradiation test modules. This module, whose dimensions are approximately 1" x 1" x ¼", contains 160 Mbits of DRAM in a dual 5 high active plus 1 spare die stacks.

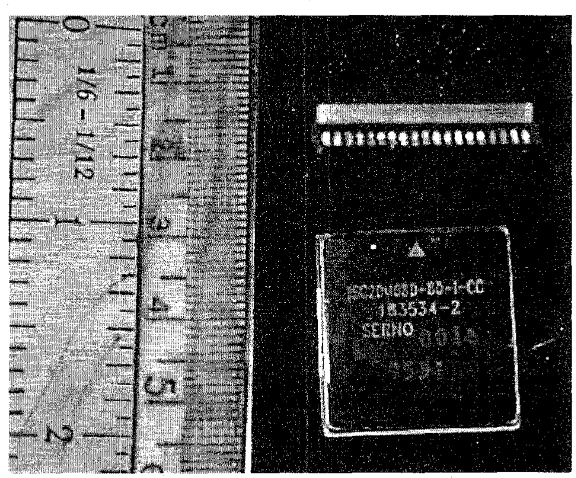

Figure 2: ISC 160 Mbit DRAM Module

B. Description of Anomaly

The HST SSR utilizes a very powerful error detection and correction (EDAC) encoding scheme known as Reed-Solomon (RS) [1]. This particular version of RS encoding is able to correct up to 10 bytes in error in a 224 byte data

* Many other versions of IBM 16 Mbit DRAMs exist including 3.3V versions. Some have built-in error correction codes (ECC) such as the Luna C devices, and some have different feature sizes (e.g., DD4 process). Many of the issues discussed herein may apply to these other versions, but the emphasis of this paper is this particular Luna ES die version.

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structure. The encoding allows for a routine single event upset (SEU) such as a single bit flip or even a multiple bit upset (MBU) to be fully correctable.

Two anomalous events occurred on the SSR during the first nine months after it was installed. Each event had a similar signature in that it produced approximately 100 correctable EDAC errors in a timeframe. The errors were correctable by the RS EDAC, indicating occurrence of a single event. These errors were not cleared by writing new data to the erroneous locations as would be expected in the case of a transient error such as a traditional bit flip. The two events occurred in different logical memory block ranges and have been isolated to two individual row addresses. It is suspected that both events could be traced to an individual die, however, in-flight engineering experiments are not HST's main purpose so further error isolation tests have not been performed.

II. Pre-Flight Single Event Effect Test Results

Initial single event effects (SEE) testing was performed with heavy ions and protons on IBM Luna ES Rev. C 5.0V die from the HST flight lot [2]. The heavy ion test results indicated an error condition similar to those observed in-flight on the HST SSR, i.e., a block of bad memory locations within a single die. The threshold linear energy transfer (LET_{th}) for zero upsets is 5 MeV-cm^2/mg. The block error conditions were removed by cycling the power or by resetting the device, but could not be cleared by re-writing the locations with new data. These heavy ion induced events were described previously [2]. They may be viewed as a type of single event functional interrupt (SEFI) [3]. Further details of this condition will be discussed with the new test results in Section III.C. SEE data on similar devices have also been presented previously [4], [5]. Predicted block SEFI error rates for HST's heavy ion component were very small (< 1 per 200 years for the entire SSR). HST's orbit (28.5 degrees, 600 km circular) does pass through the South Atlantic Anomaly (SAA) which contains high energy trapped protons.

The type of SEFI observed on the IBM DRAM is most likely due to an error in a redundancy latch that is internal to each die [6]. Each die contains redundant rows and columns. When the device is first powered up, weak (those where the data retention of the cells is suspect) or bad (those where bits are always incorrect) rows and columns are replaced with redundant row and columns. A redundancy latch that maintains the device's configuration (i.e., which rows and columns have been replaced) is programmed by laser cuts and is initialized upon power up. The row or column replacement is performed in order to improve the product yield. A single particle strike can affect this configuration circuit. When this "event" occurs, a weak or bad row or column may get placed into the device configuration. To remove the anomalous condition, a reset or power cycle must be initiated to place the device in its correct configuration.

One would also expect proton-induced SEEs because of the low LET_{th}. However, proton SEE testing of three die provided a mixed result: no block SEFIs were observed. The implication is that these IBM DRAMs have a low sensitivity for block SEFI occurrence (i.e., limiting cross-section of $<2\times10^{-12}$ cm^2/die). However, with a SSR design that uses 1440 devices, the test fidelity with a sample size of three (even with overtest conditions) must be questioned. Because no events were observed with the proton test, the HST program deemed the SEFI problem a non-issue for their mission. The project chose to proceed with the uncertainty associated with the concept of a limiting cross-section.

III. Proton Tests of the IBM DRAM

The HST project has initiated investigations into the cause and possible impact on space system performance from the in-flight anomalies. One issue to resolve was the question of proton-induced events on the DRAMs, therefore, it was decided to perform further proton testing.

A. Proton SEE Test Plan

A new test plan aimed at simulating a 1440 die SSR in the HST orbit was designed. The goal was to perform a better prediction of the nature of the in-flight anomaly and the rate occurrence. With the large size of the memory, the question was, "how many devices must be irradiated to perform an adequate test?" The expected proton fluence for $E > 25$MeV for the HST orbit is $\sim3\times10^9$ p+/cm^2/year behind 100 mils of Al shielding. With two events occurring in approximately nine months, we would expect a cross-section on the order of 6×10^{-13} cm^2/die. The observed rate depends on the percent of the SSR memory being scrubbed by the EDAC and is most likely approximately 75% of this number. Thus, in order to gain sufficient statistics, it was decided to irradiate 100 of the DRAM die. The availability of so many devices was an issue. However, with the suspected anomaly being die-related and not packaging-related (i.e., a single particle affecting multiple die), the package configuration was not deemed critical for this series of experiments. Therefore, DRAM die packaged in 10 ISC 160 Mbit modules were used even though the module configuration is different from the HST's flight SSR (dual 5 high stacks versus dual 10 high).

It was also important to irradiate the DRAMs with an overtest proton fluence to gain adequate statistics. Knowing the device's total ionizing dose (TID) tolerance based on previous Co-60 irradiations (~25-30 krad (Si)), a fluence of 1.5×10^{11} p+/cm^2 (delivered during three test runs) using 63 MeV protons was chosen. This is approximately 20 krad (Si). Thus, based on the assumed die cross-section from the flight data, we would expect a single anomaly occurrence during the ground irradiation for every module or device under test (DUT), i.e., approximately 1 per 10 die at the given cumulative test fluence. Particle flux rates were held such that error rates were less then one per second.

The ISC modules obtained for this experiment were from two separate lot date codes (LDCs) (9533 and 9531). The actual LDCs for the IBM die are unknown.

B. Test Facility and Test Method

Ground irradiations were performed at the University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL). This facility provides monoenergetic protons with a maximum energy of 63 MeV incident on the device package. It is understood that the space environment has a wide spectrum of proton energies, but through the use of proper prediction tools, relatively accurate in-flight predictions may be obtained by testing with a single energy. Additional tests were performed on two additional DUTs with 193 MeV protons (Indiana University Cyclotron Facility or IUCF). The preliminary results of the IUCF tests are consistent with the results of the 63 MeV experiment at Davis. This data set has not been included here because the analysis is not yet complete.

We have calculated the energy distribution through the stacked DRAM package for the case of the 63 MeV proton test energy. In all cases, the protons were normally incident on the lidded package. Approximately 5 MeV was lost in the KOVAR lid, and the deposition in the 50 mil thick die resulted in incident energies at the respective die positions of 58 MeV, 55 MeV, 53 MeV, 50 MeV, 47 MeV, and 44 MeV. Note that the packages used for testing were comprised of twelve die in two stacks of six die each. Of these six die per stack, only five were active. At present, we do not have a mapping of the error locations within the stack. We recognize that the cross section has some energy dependence, however this would not be expected to be extreme over the range from 44 MeV to 58 MeV. For our purposes, the incident energy could be described as 50 MeV with an uncertainty of 8 MeV. Note that this also accounts for energy straggling at the lower average energy of 44 MeV. For the case of 193 MeV protons, these issues hold even less importance.

Each module was tested using GSFC's VXI-based test system. Devices were tested and operated in one of three manners during irradiation:

- The device was loaded with a test pattern prior to irradiation with row address (RAS) refreshing performed during irradiation (64 msec refresh cycle). DUT data were read by the test system post-irradiation and compared to the known data test pattern.
- During irradiation, the DUT was operated in byte access mode with a read data – modify if in error – write correct data (RMW) cycle of 900 nsec per byte. And,
- During irradiation, the DUT was operated in page access mode with RMW cycle of 900 nsec per byte.

Data such as address and incorrect data values were collected for each run for post-test analysis. Block SEFIs were identified during irradiation by the large "jumps" in error counts that could not be corrected without a device power cycle or reset.

The test pattern utilized was a checkerboard (alternating 1's and 0's) that was reversed after each DUT access cycle. All tests were performed at room temperature (23°C) with a nominal 5.0V power supply voltage. While it is understood that SEU sensitivity tends to increase with reduced power supply voltage, the flight project set nominal condition testing as a requirement.

C. Details of Proton SEE Test Results

Many different SEE error conditions were observed. They included:

- block SEFIs, where an entire (or a large portion) of a die row or column became in error and required a device reset or power cycle to clear;
- temporary block errors, where re-writing data to these blocks would clear the error;
- single bit errors;
- (logical) multiple bit upset (MBU) errors (We did not have a die map, so mapping physical MBUs was beyond the scope of this effort.), and;
- stuck bits or single hard errors, where a single bit had a "stuck at" value that could not be cleared.

No statistical variation was observed due to operating or test mode.

Cross-sections were calculated by N = x F, where N is the number of events observed and F is the particle fluence.

1. SEFI Block Errors: A total of 9 events were observed that had similar characteristics to the in-flight HST anomaly. With 1 event to every 11.1 die irradiated, this is roughly the same as the approximately 1 in 10 expected based on the flight data. In addition, 2 types of block SEFI were noted:

- a bad or failed column in a die where stored values are always in error and
- a weak column in a die where the data stored is sometimes in error (but sometimes valid).

These errors are consistent with the expected hit to the redundancy latch in a single die swapping bad or weak memory areas for good ones. All of these events were removed by power cycling or a device reset. The failed column cross-section is ~ $5.06\text{x}10^{-13}$ cm^2/die, while the weak column error cross-section is ~$6.33\text{x}10^{-14}$ cm^2/die.

2. Temporary Block Errors: The temporary block errors were correctable by writing locations in error with new data. Events were observed that affected either rows or columns, but no events caused errors in both. Cross-sections for these errors are $7.25\text{x}10^{-13}$ cm^2/die for row errors and $8.84\text{x}10^{-12}$ cm^2/die for column errors. A possible cause of temporary block errors is a single particle strike which produces an upset in an internal address pointer register causing a block of addresses to be "skipped" during a device operation (refresh, read, or write).

3. Single Bit Errors: The traditional single event upset (SEU) of single memory cell flips occurred on every test run with a cross-section of $5.57\text{x}10^{-17}$ cm^2/bit.

4. (Logical) Multiple Bit Errors: Only one logical bit error was noted during testing. Without the use of a physical-to-logical device map, it is unknown as to whether this event was caused by a single particle hit. The measured error cross-

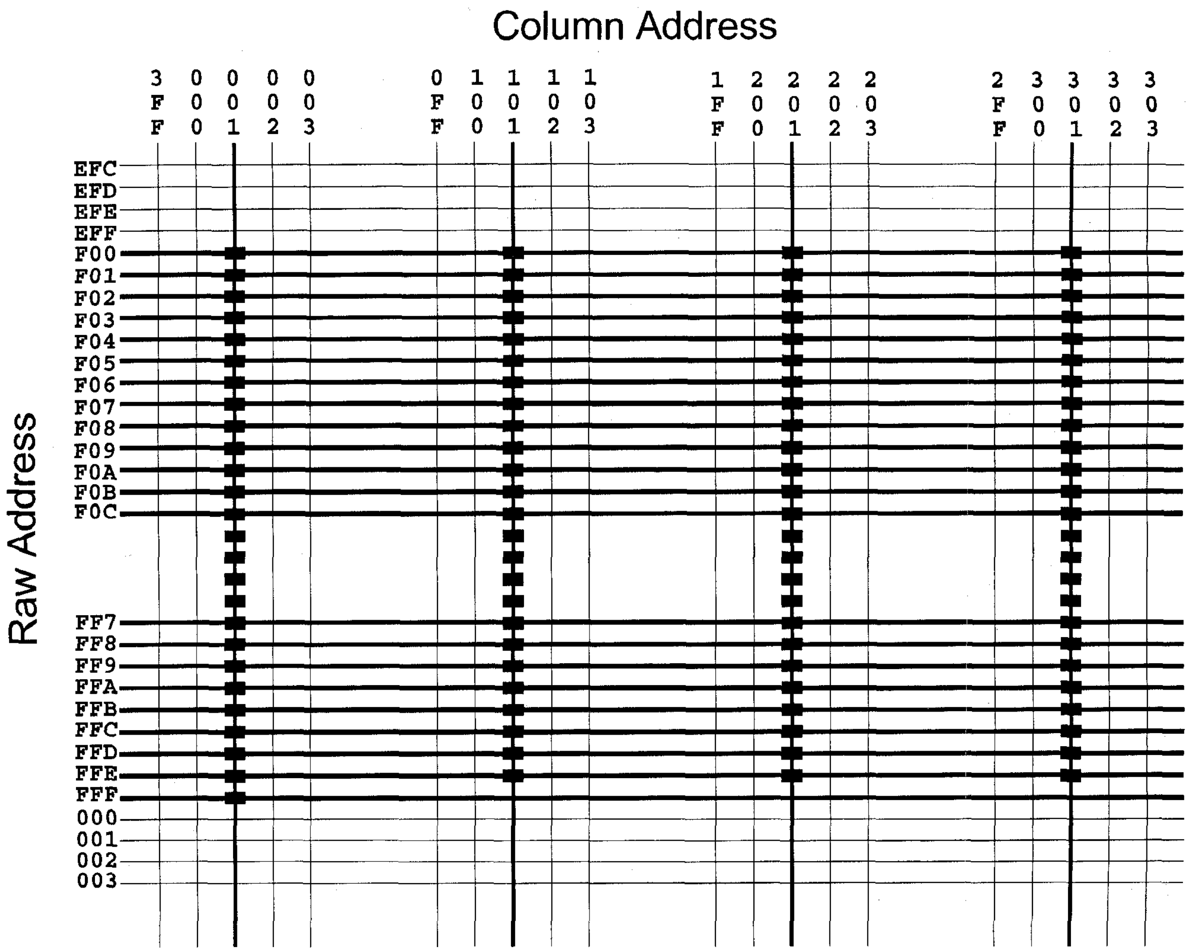

Figure 3: An illustration of a block SEFI mapped to the logical address space of a die (IBM Luna ES Rev. C DRAM). Darkened areas indicate the occurrence of errors. In this case, whenever the column address in this page of die memory had a value of x01H, the data was in error.

section is 1.5×10^{-20} cm^2/nibble (remembering that each die is in a x4 configuration).

5. Stuck bits: Seven single bit hard errors (or bit fails) were observed during the radiation experiments. These were logical address locations where a single bit of the nibble could not be re-written with a different value. Power cycling or device resets were unable to remove this condition. Investigation of the cause of these bit fails is currently underway, but the events do not appear to be enhanced by the cumulative total dose placed on the device. Multiple causes are being considered including microdose, single event gate rupture (SEGR), total dose effects, etc. [7]

IV. Correlation of In-Flight Anomaly and Ground Test Results

The in-flight anomaly symptoms appear very similar to a failed column error. Based on the measured error cross-section and the predicted radiation environment, the in-flight anomaly rate for this type of SEFIs would be 2.2/year for the HST SSR. This is the same order of magnitude as the observed in-flight rate of two in nine months. It should be noted that the error bars for the in-flight prediction are rather large (factor of 2 or more). This is due to:

- the small number of anomalies observed during ground testing (9 in 100 die),
- the actual proton environment at the die level (probably >100 mils effective Al shielding), and,
- the actual percent of SSR memory in use (an error could occur in an unused portion and it would not be discovered until that block of memory is accessed).

V. Additional Ground Test Data Examples

Two antifuse-based field programmable gate array (FPGA) devices were also investigated for low sensitivity to proton-induced events: the Actel A1280A and RH1020 devices. The A1280A device has been characterized by multiple organizations for its SEE sensitivity to heavy ions and protons. [8], [9] To date, errors on the S (or sequential) logic modules have not been observed on small sample sizes with protons despite a LET_{th} for zero upsets between 3 and 5 MeV-cm^2/mg. This would clearly indicate a probable proton sensitivity. Thus, an experiment was planned to irradiate a larger sample size (18 devices) with protons in a test configuration with 522 S-modules utilized per sample.

All of the A1280A devices were from the Matsushita Electronics (MEC) foundry with a 1.0 um feature size. Devices from four separate LDCs were utilized ranging from 9415 to 9614. DUTs were tested with a 1 MHz clock and a 500 kHz square wave input. Tests were performed with both 4.5 and 5.0V power supply voltages and at room temperature. Previous limited published proton test data on a small sample size did not exhibit S-module sensitivity [10]. A previous small sample test by GSFC noted a few sporadic S-module proton upsets, however, because of the poor statistics (two errors in four device samples at low fluences) of that test, this higher sample size test was initiated at IUCF.

Eleven A1280A samples from four differing LDCs were tested with a 4.5V power supply voltage. The average cross-section measured with 193 MeV protons was 1.36 +/-0.4x10^{-13} cm^2/S-module flip-flop. The additional seven samples tested at 5.0V had an average cross-section of 1.25 +/-0.44x10^{-13} cm^2/S-module flip-flop. Variance by LDC at either supply voltage was negligible.

The Actel RH1020 is fabricated using Lockheed-Martin Federal System's TID hard CMOS process. Unlike the A1280A that has sequential (S) and combinatorial (C) logic modules as well as limited input/output (I/O) modules, the RH1020 only has C-modules. Two lots were characterized: a pre-production lot (5 samples) and a production lot (3 samples) that included improved clock buffer circuitry and a slight thinner antifuse. Because of the known TID hardness (>100 kRad(Si)), higher fluences per device sample were utilized than with either the A1280A or ISC DRAM stack irradiations.

The test setup for the RH1020 is essentially the same as for the A1280A with the irradiations performed at room temperature and at both 4.5 and 5.0V power supply voltages. For the eight samples irradiated, a total of three upsets on the C-modules were noted: 1 at 4.5V (3 samples), 2 at 5.0V (5 samples). The error cross-section at 4.5V was 1.8x10^{-15} cm^2/C-module flip-flop, while at 5.0V the cross-section was 1.5x10^{-15} cm^2/C-module flip-flop. Obviously with such poor statistics (1 and 2 upsets per LDC), no discernible differences between lots of the RH1020 can be determined. As a note, no clock distribution events (which manifests itself during test runs as a burst of errors) or antifuse damage were observed during any of the RH1020 irradiations.

VI. Discussion

The results of the testing and the in-flight experience emphasize two important points from an applications perspective. Fault-tolerant system designs are required to mitigate anomalies such as those observed by the HST SSR. Second, to simulate space usage where large numbers of die are used or critical functions are performed, statistically significant ground tests must be performed.

The authors would like to point out that HST has lost no science data due to the in-flight SSR anomalies. The use of a robust RS EDAC scheme allows for full system operation despite single device issues. Best estimates indicate that no lost data would occur from these radiation-induced anomalies (assuming the predicted event rate) during the HST SSR's mission lifetime (>7 years). For this reason, power cycling is not planned. This would not be the case if the scientists were in danger of losing data. Resets of the devices are not feasible since this capability does not exist in the current SSR memory controller design. However, during the installation of a second SSR (another 1440 of the same die) in an upcoming service mission, power will be cycled, thus minimizing the block SEFI conditions. In addition, after the second SSR installation, we will increase the sample size of devices for gathering in-flight data.

The other types of events noted during ground test irradiation are of no lesser concern. However, a smart EDAC system such as RS encoding can mitigate these types of events (single bit, multiple bit, temporary block, and stuck bit errors). It has been pointed out that single hard errors have been observed on memory devices [11] and it is possible that they may eventually be observed on other types of devices. If these hard errors were to occur in a microprocessor, for example, the mitigation required to ensure system functionality would not be so straightforward. One must look carefully at the utilization of such devices. Knowing the risks (i.e., device radiation sensitivity) along with good engineering skills allows for successful system operation in space. This is not always so, and each application must be evaluated on a case-by-case basis. In this instance, designing the ability in the SSR memory controller to reset these devices would have been prudent.

The second concern is providing statistically significant data. Flight programs do not always want to spend the money to evaluate a sufficiently large sample size. More than one flight program has learned this lesson the hard way. The example of the HST SSR illustrates this clearly. The program initially relied on a limited set of initial data. When more extensive data were gathered, a more realistic event rate was determined. If a single sample of a device type is being utilized in a space mission, ground irradiations on three to five test samples may be sufficient. However, the larger the number of die used in flight, the larger the ground irradiation sample size required.

It is also important to pay attention to the total dose tolerance of devices during their test planning. Unlike total dose hard devices such as the RH1020 where high fluences may be safely used for SEE tests, the A1280A fails at relatively low dose levels and more samples are needed to perform ground irradiations to simulate in-flight low probability events.

The testing of the Actel A1280A's indicates two further lessons. The first concerns testing significant portions of an IC, i.e., having sufficient S-modules in the test circuit. For example, with less than 100 S-modules and lower test fluences, this low probability event may be missed and in this case it was.

The RH1020 test results showed that even when moderately large test sample sizes and high (re: overtest) fluences are utilized, statistics may be poor. Unless large numbers of these devices are utilized in a space mission, the probabilities are very small of anomaly occurrence due to proton upsets on this device type.

In the instance of the stacked DRAMs, the packaging of the die is not the prime concern for the anomalies noted. The authors would note the concerns surrounding secondary particle formation from packaging materials (or die) or multiple die strikes from a single particle. However, the in flight anomaly occurred on a single die in each module and does not appear to be packaging related.

VII. Summary

We presented a description of an in-flight HST SSR anomaly as well as SEE ground test data for the potentially error-causing device. A probable correlation was determined between the ground and flight data including identifying a possible target on the die to cause such an event. Further data were presented on two additional device types. These data sets illustrate the need for larger sample sizes as well as the potential for device reliability features such as a redundancy latch to introduce new failure modes. With only three DRAM die previously proton characterized, performing a statistically significant test to simulate 1440 die becomes important.

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